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38	Power Sequence	1A	

PCB STACK UP  
6L

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

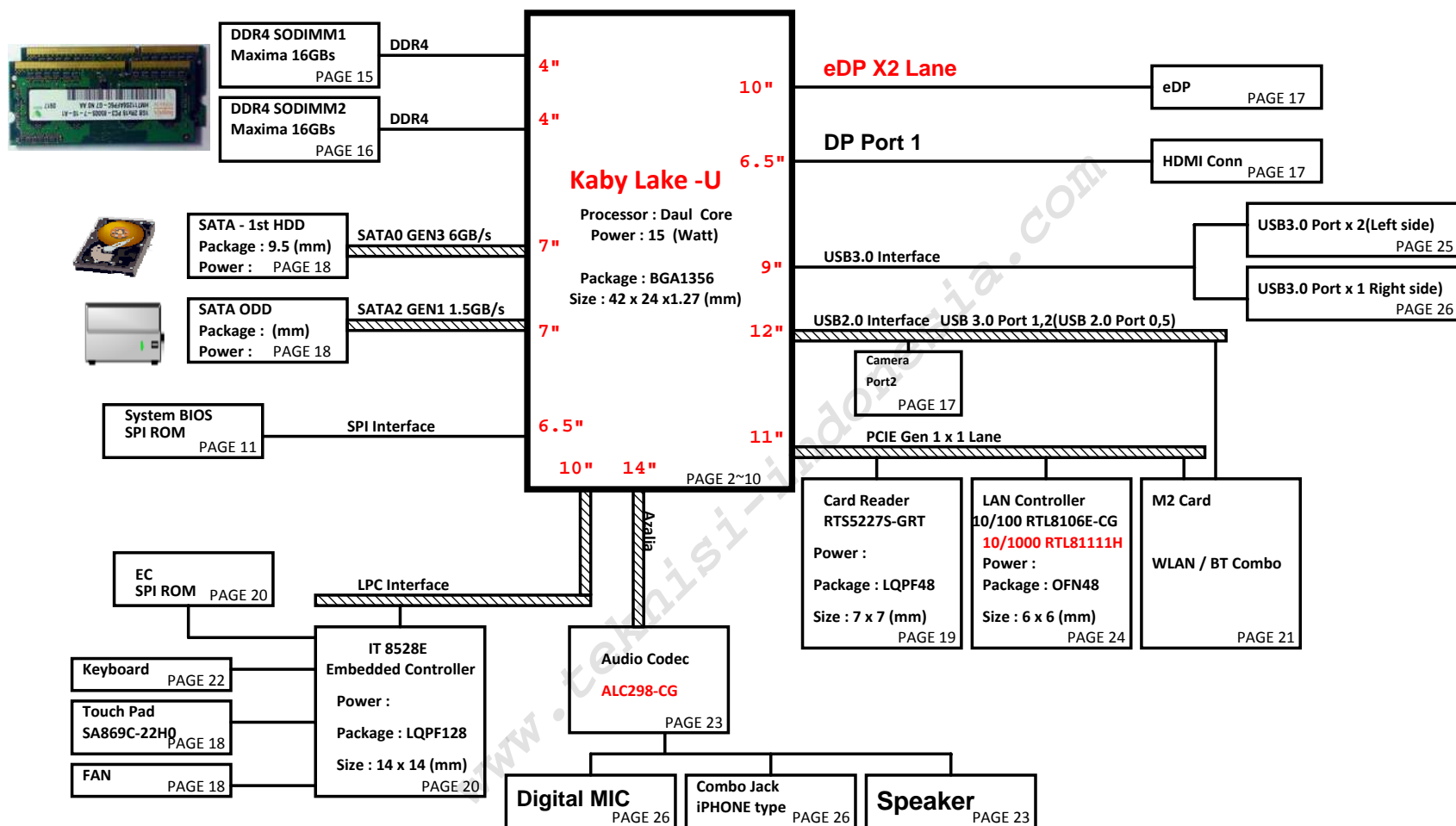
BOM select

XDP@: XDP
* : No mount

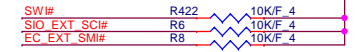
F/W List

	Location	Update method
BIOS/ME	U3	Flash tool in Windows
EC	KU4	Flash tool in Windows

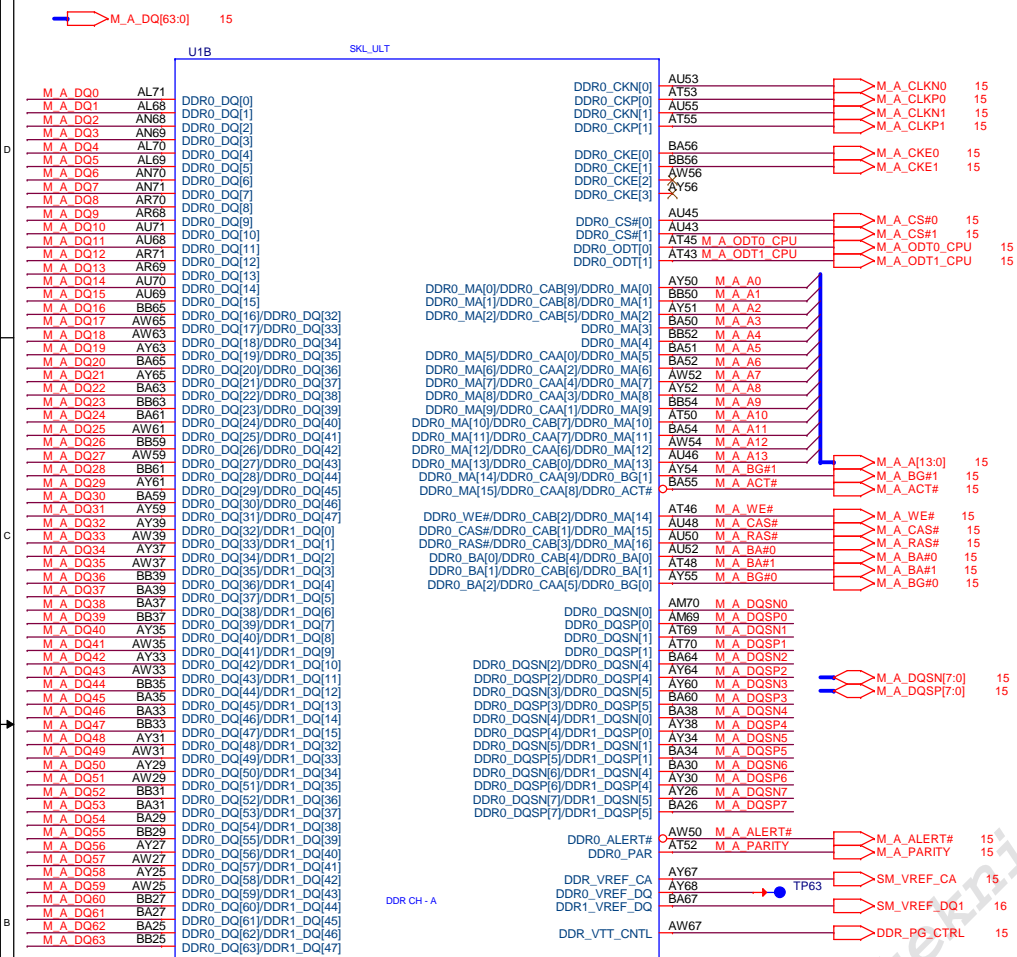
# FFK 15.6" Ultra/Slim Intel Kaby Lake U Platform Block Diagram



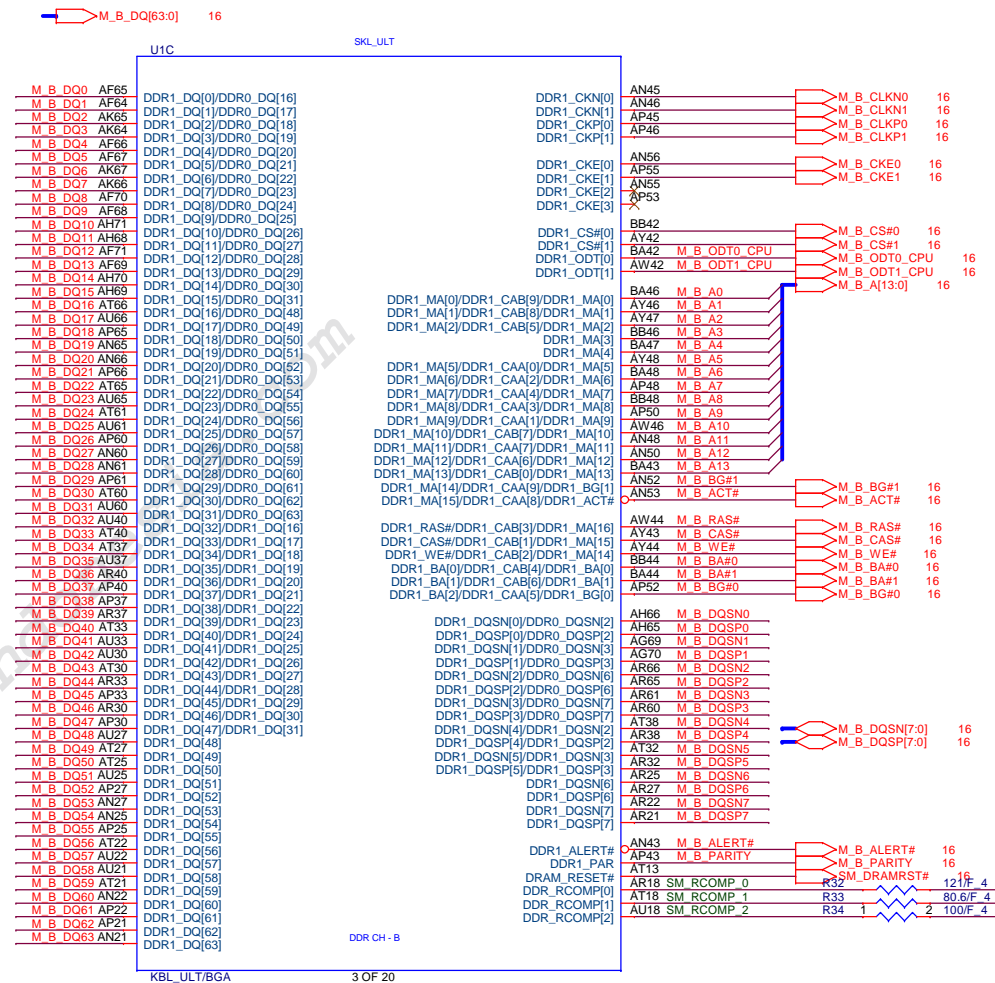
REV	CHANGE LIST							
ES2	1 AR26, R5164, R5165, R5166, R5167 change to short pad							
	2 CN27 2IN1 CARD change to footprint sdcard-psdbtm-09glbs1nn4hb-smt for correct							
	3 Change EMU_LID GPA5 to GPH1 (Open Drain) for BLON timing.							
	4 Stuff C597 0.01uf for VCCST_PWRGD understood issue.							
	5 Add KR83, KU6 & KC36, KC37 circuit location for tPLT18 timing issue with reserve							
	6 Stuff PR327 & PQ61, MAIND change to RUN_ON for tPLT18 timing issue.							
	7 change PR34 from 137k to 124k ohm to correct IMON							
	8 change PR11 from 2.26k to 1.96k to correct LL							
	9 change location PR1,PR2,PR36,PR37,PR53,PR55,PR352 to short pad from 0 ohm 0402 resistor for ES2 stage.							
	10 Del location PG1, PG18, PG14, PG15, PG16, PG17, PG2, PG8, PG13, PG3, PG10, PG9 and PG12, ER13 short PAD for FFK ES2 Verify schematic.							
	11 PC126 change to 220pf from 2200pf & PC121 change to 680pf from 560pf for audio sequence issue.							
	12 PC35 from 680pF to 1000pF to correct DVID reponse							
	13							
	14							
PP	1 Change PR180 0ohm to 100kohm & stuff PC142 0.01uF RC delay timing for meet +1.2V_SUS & +2.5V_SUS sequence timing							
	2 change PR48 from 4.32k to 6.8k ohm to correct DCR error at high temp .							
	3 change PR49 from 316 to 365 ohm to set Min 44A OCP							
	4 change PR30 from 110k to 118k ohm to correct IMON.							
	5 change PR10 from 4.32k to 6.8k ohm to correct DCR error at high temp .							
	6 change PR11 from 1.96k to 2.1k ohm to correct LL.							
	7 change PR5 from 316 ohm to 340 ohm to correct LL and IMON.							
	8 change PR42 from 1.65k to 1.78k to correct LL							
	9							
	10							
	11							
	12							
	13							
	14							
	15							
	16							
	17							
	18							
	19							
MRT	1							
	2							
	3							
DOC NO.		PROJECT MODEL :	FFK	APPROVED BY:		DATE:	2016/10/18	
		PART NUMBER:		DRAWING BY:		REVISION:	3A	



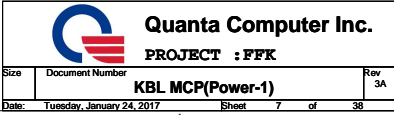
## KabyLake ULT (DDR4)

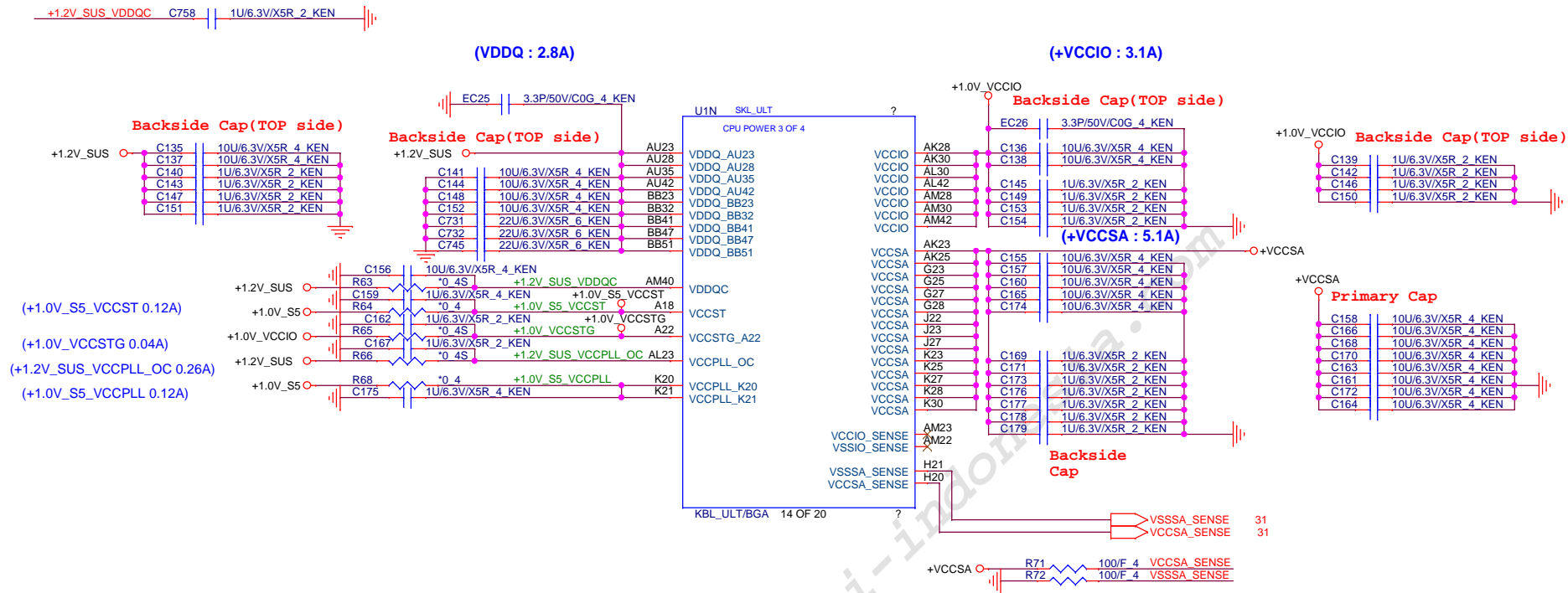


KabyLake ULT (DDR4)



	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG4 eDP enable:	DISABLED	ENABLED	





For Debug mode:+1.0V\_VCCSTG will use +3V\_S5 power rail

For Load switch <=65usec full load ready

+1.0V\_S5 R514 \*XDP@0.4 +1.0V\_VCCSTG

+1.0V\_SUS\_VCCST R472 \*0.4S +1.0V\_S5\_VCCST  
R473 \*0.4S +1.0V\_S5\_VCCPLL

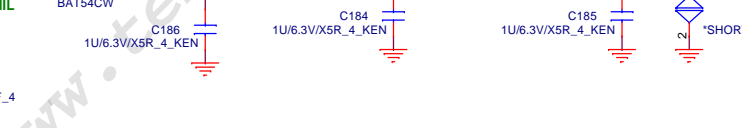
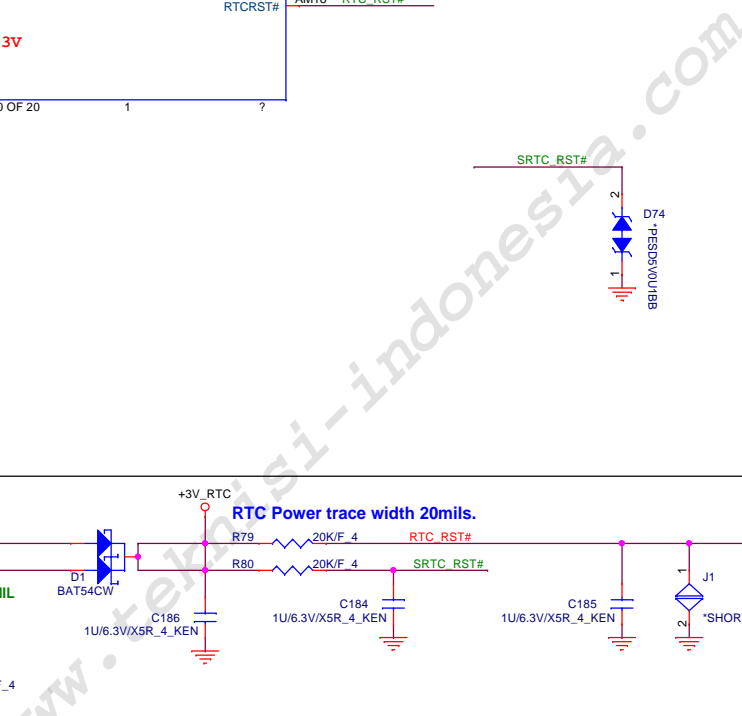


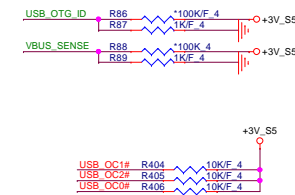
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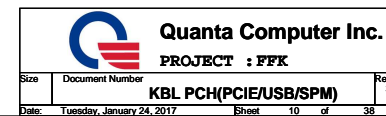
Size Document Number Rev 3A  
KBL PCH(Power-2)  
Date: Tuesday, January 24, 2017 Sheet 8 of 38







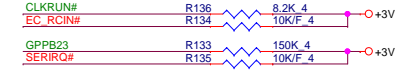
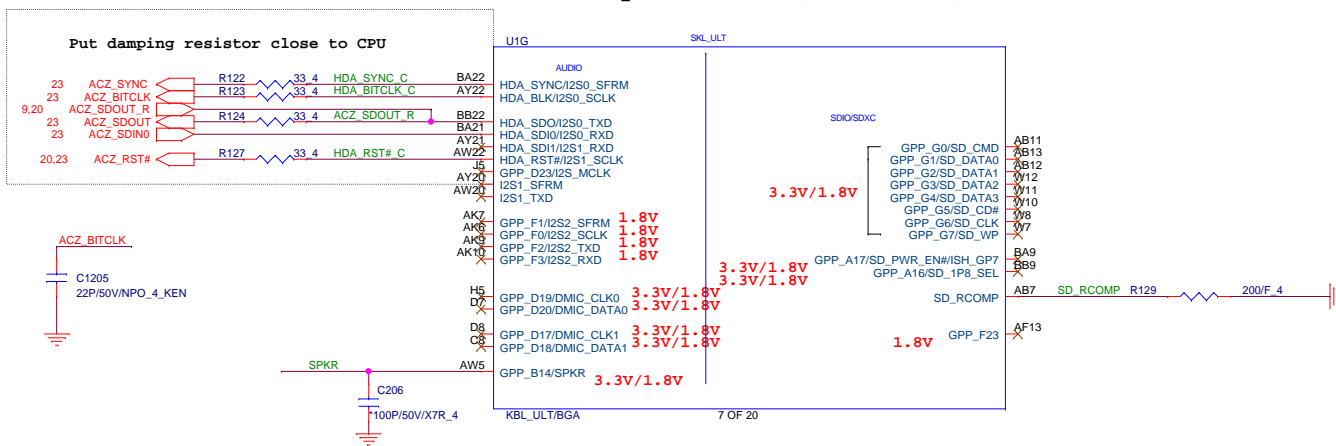
PCH Pull-high/low(CLG)



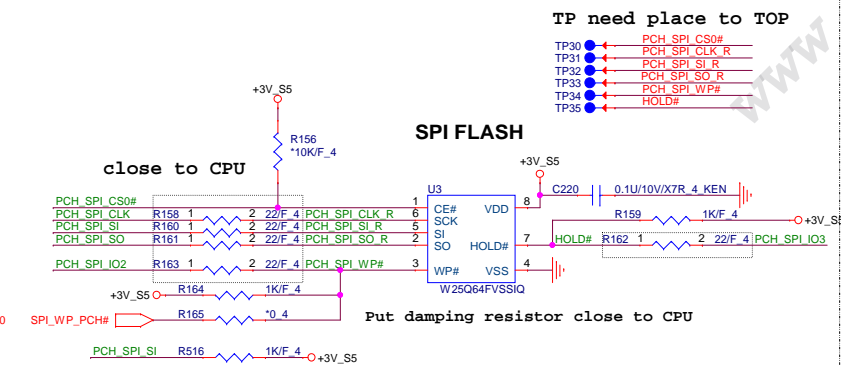
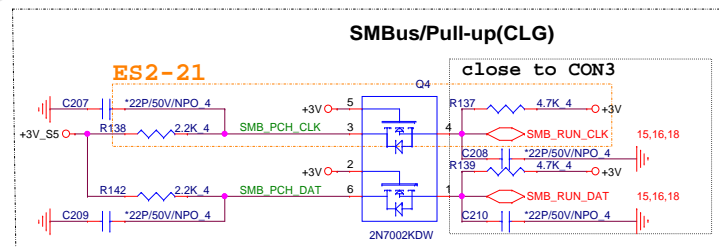
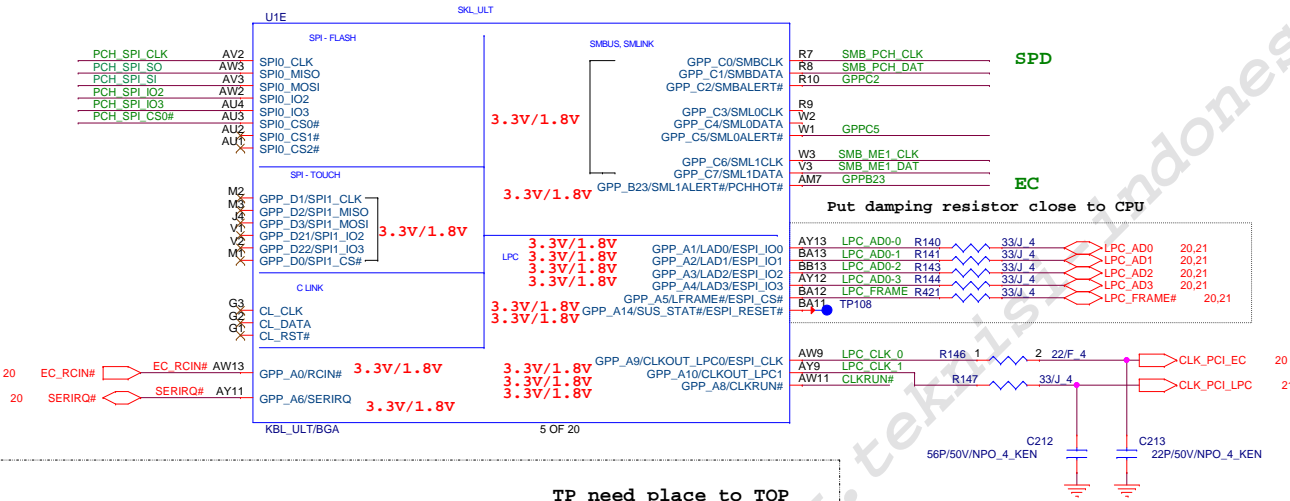
# KabyLake ULT (HDA/SDXC)

GPCC5: ESPI or LPC SEL  
HIGH: ESPI interface  
LOW: LPC interface(default)INT DN

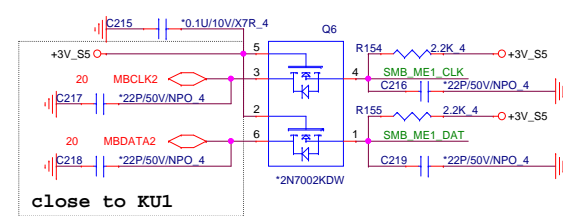
11



## KabyLake ULT (LPC/SPI/SMB/CLINK)



TLS CONFIDENTIALITY STRAP (GPP_C2)	
NC	Default
PU	EN



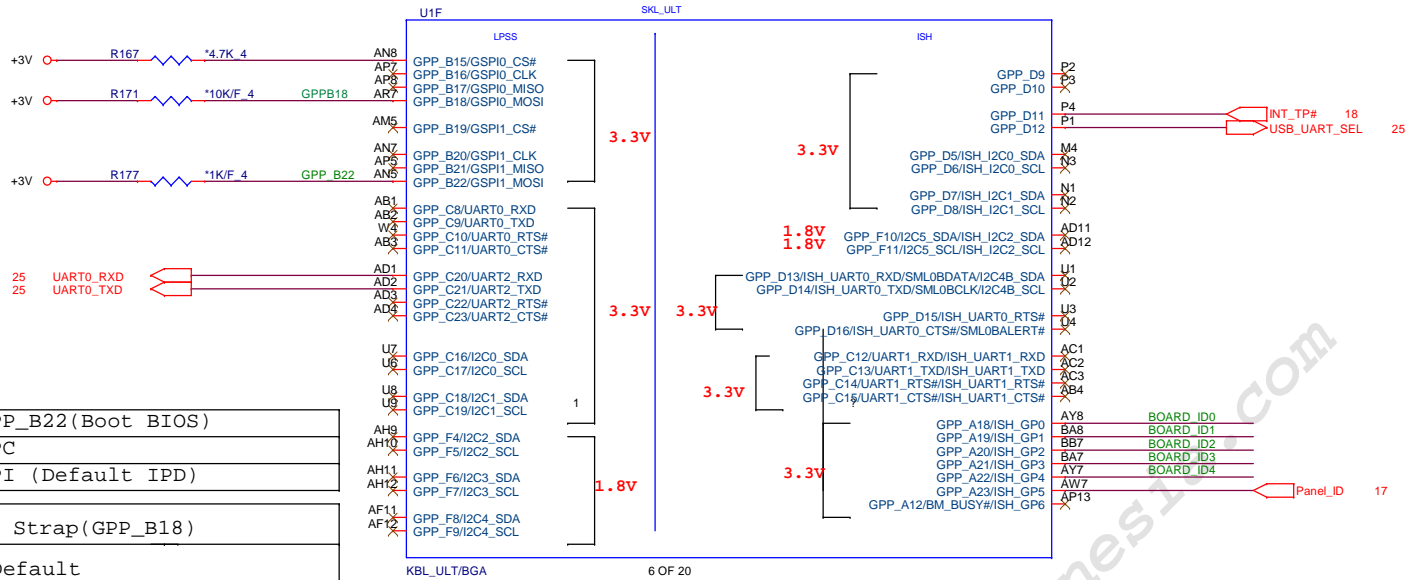
Vender	Size	P/N
MACRONIX	8MB	AKE3EZN0Z00 (MX25L6473EM2I-10G)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
Socket		DFHS08FS023

SPKR/GPP_B14 Top-Block Swap	
PU	Enable
PD	Disable(Default) internal weak pull-down

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PROJECT :FFK

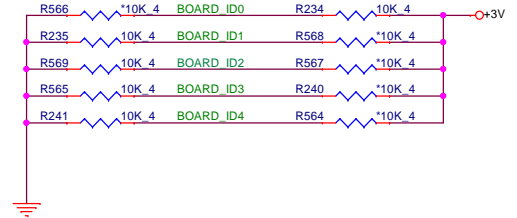
Size	Document Number	KBL PCH(HDA/LPC/SPI/SMB)	Rev 3A
Date:	Tuesday, January 24, 2017	Sheet	11 of 38

# KabyLake ULT(GPIO,LPIO,MISC)



GPP_B22(Boot BIOS)	
PU	LPC
PD	SPI (Default IPD)
No Reboot Strap(GPP_B18)	
NC	Default
PU	EN

## GPIO Pull-up/Pull-down(CLG)



## PANEL ID

PANEL ID	
H	HD
L	FHD

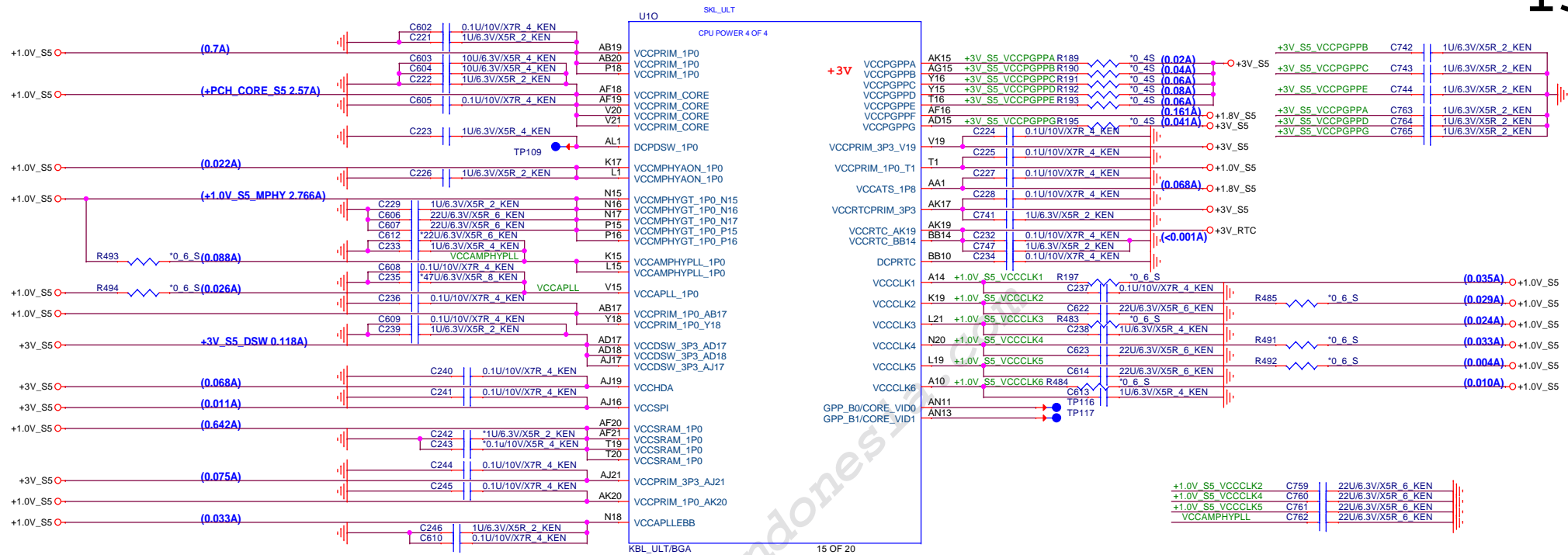
Project	CPU BGA	LAN	Web Camera	MB ID				
				BOARD ID4	BOARD ID3	BOARD ID2	BOARD ID1	BOARD ID0
FusionK-H	Celeron	GLAN	2 DMIC	0	0	0	0	1
FusionK-H	Pentium/13/15/17	GLAN	2 DMIC	0	0	0	0	1
FusionK-L	Celeron	100M	1 DMIC	0	0	0	0	0
FusionK-H								
FusionK-H								



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PROJECT : FFK

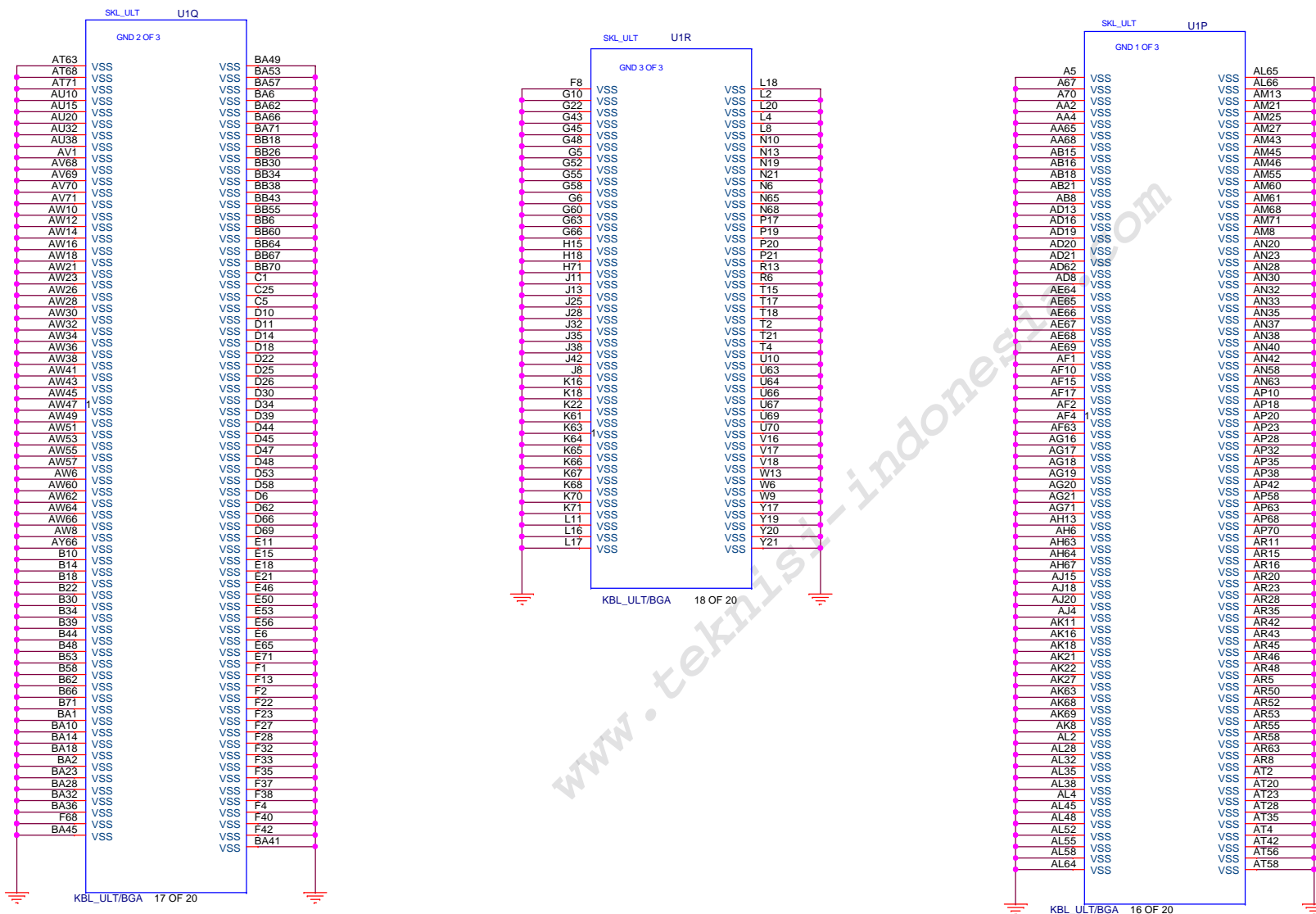
Size	Document Number	Rev
	KBL PCH(GPIO/UART/I2S)	3A
Date:	Tuesday, January 24, 2017	Sheet 12 of 38



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KBL PCH(Power)



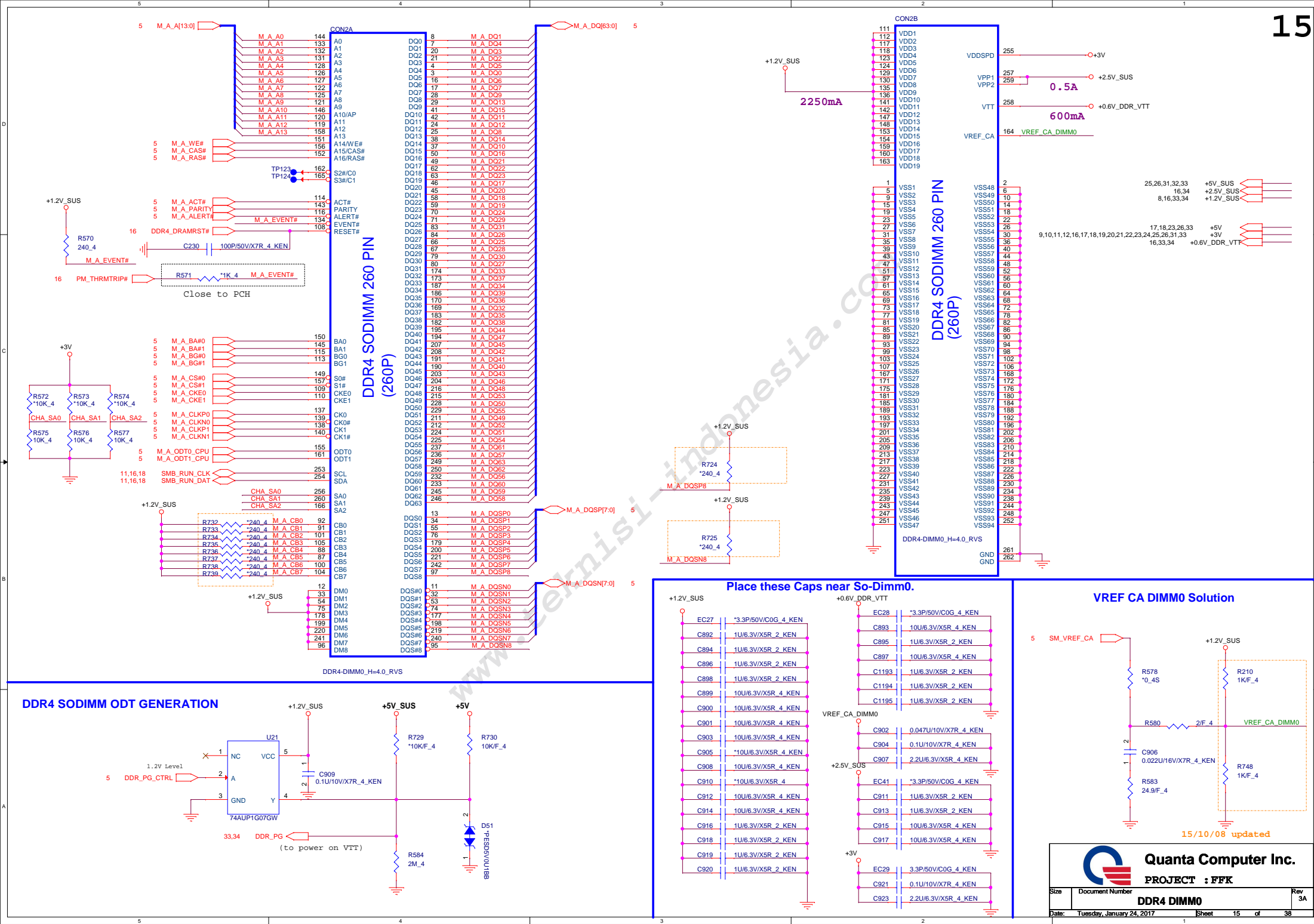
**Quanta Computer Inc.**

**PROJECT : FFK**

**KBL PCH(GND)**

Size: Document Number: Rev: 3A

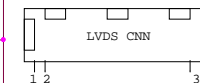
Date: Tuesday, January 24, 2017 Sheet 14 of 38



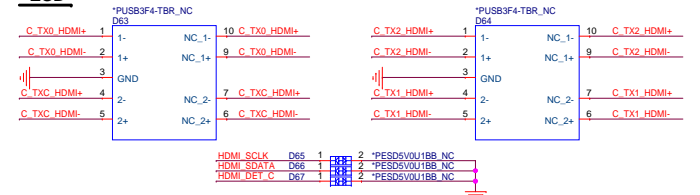
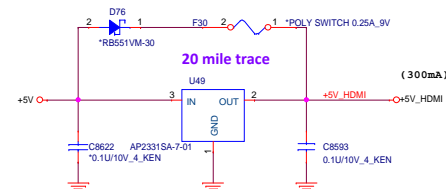
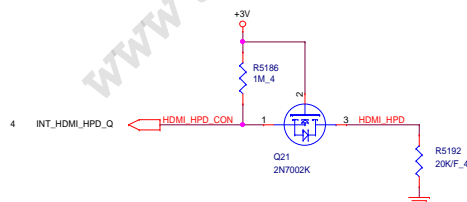
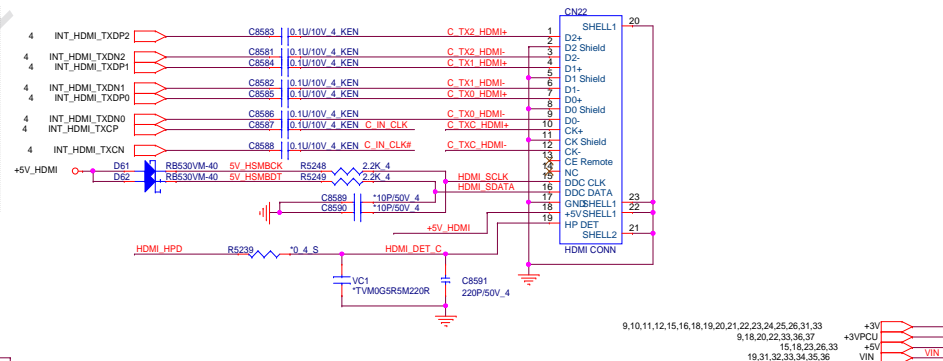




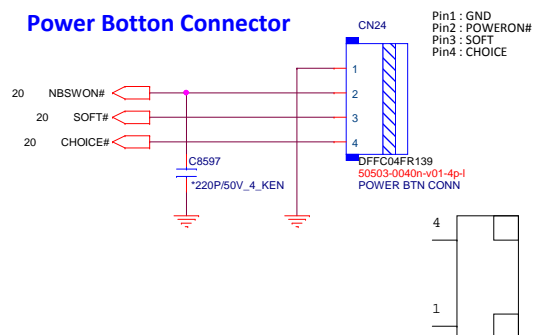




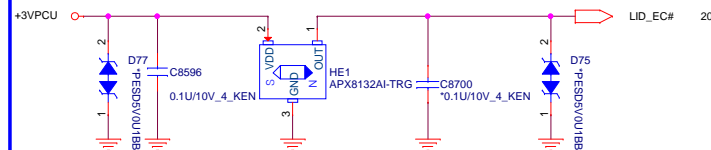
## EMI Solution 1218



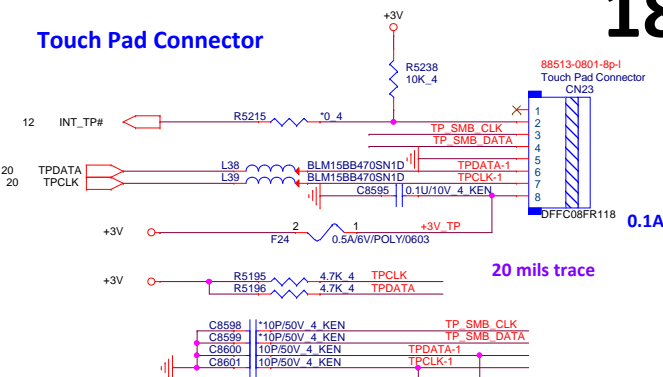
## Power Button Connector



## HALL SENSOR



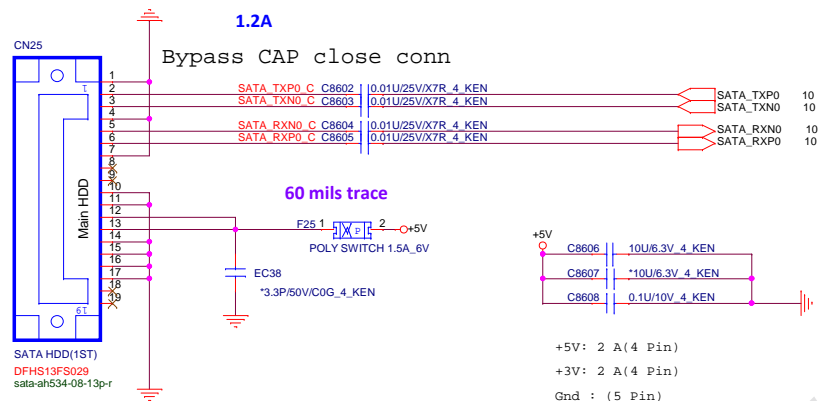
## Touch Pad Connector



20 mils trace

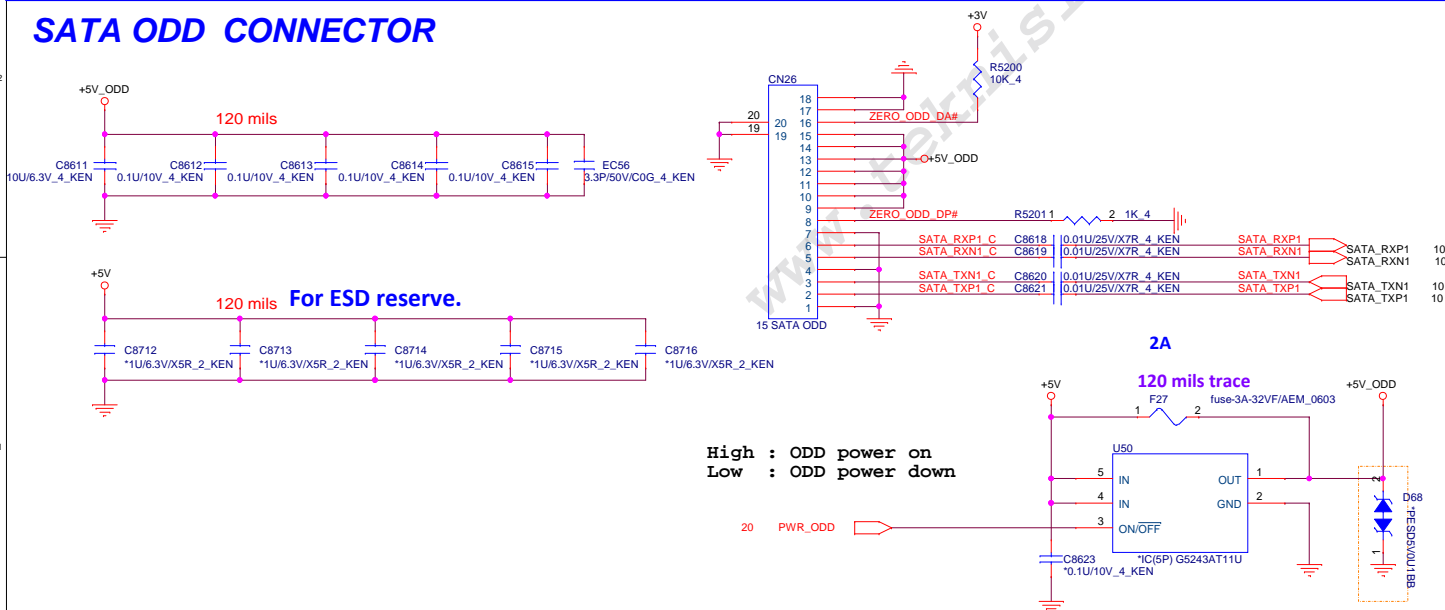
0.1A

## SATA HDD Connector(Cable type)



60 mils trace

## SATA ODD CONNECTOR



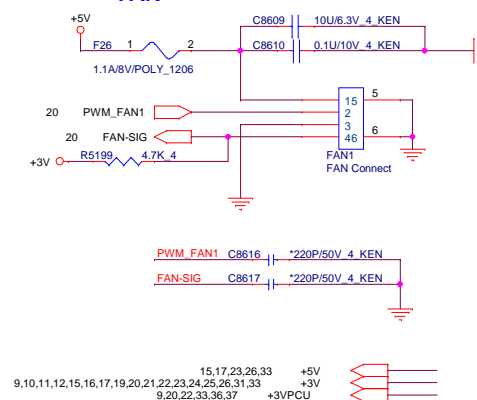
High : ODD power on  
Low : ODD power down

2A

120 mils trace

## FAN

50 mils trace



Reserve for EMI

SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

SD / MMC

9,10,11,12,15,16,17,18,20,21,22,23,24,25,26,31,33 +3V

CLOSE CONN

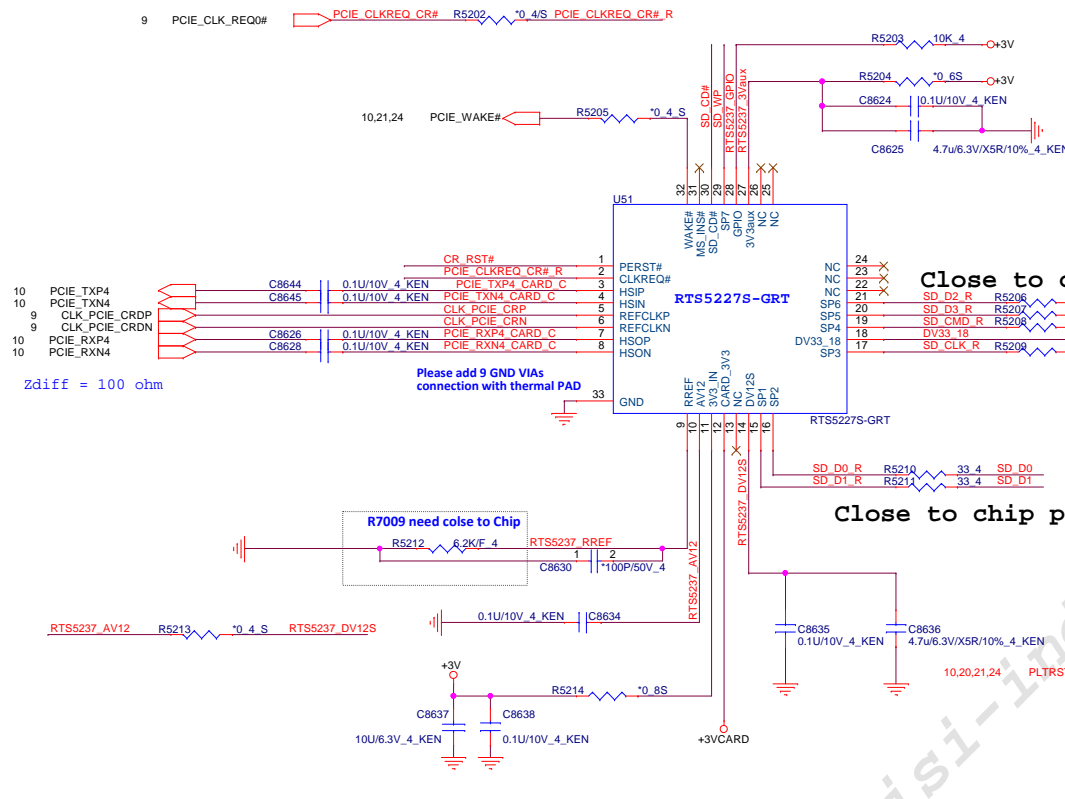
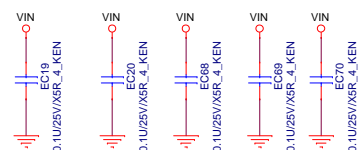
40 mils trace

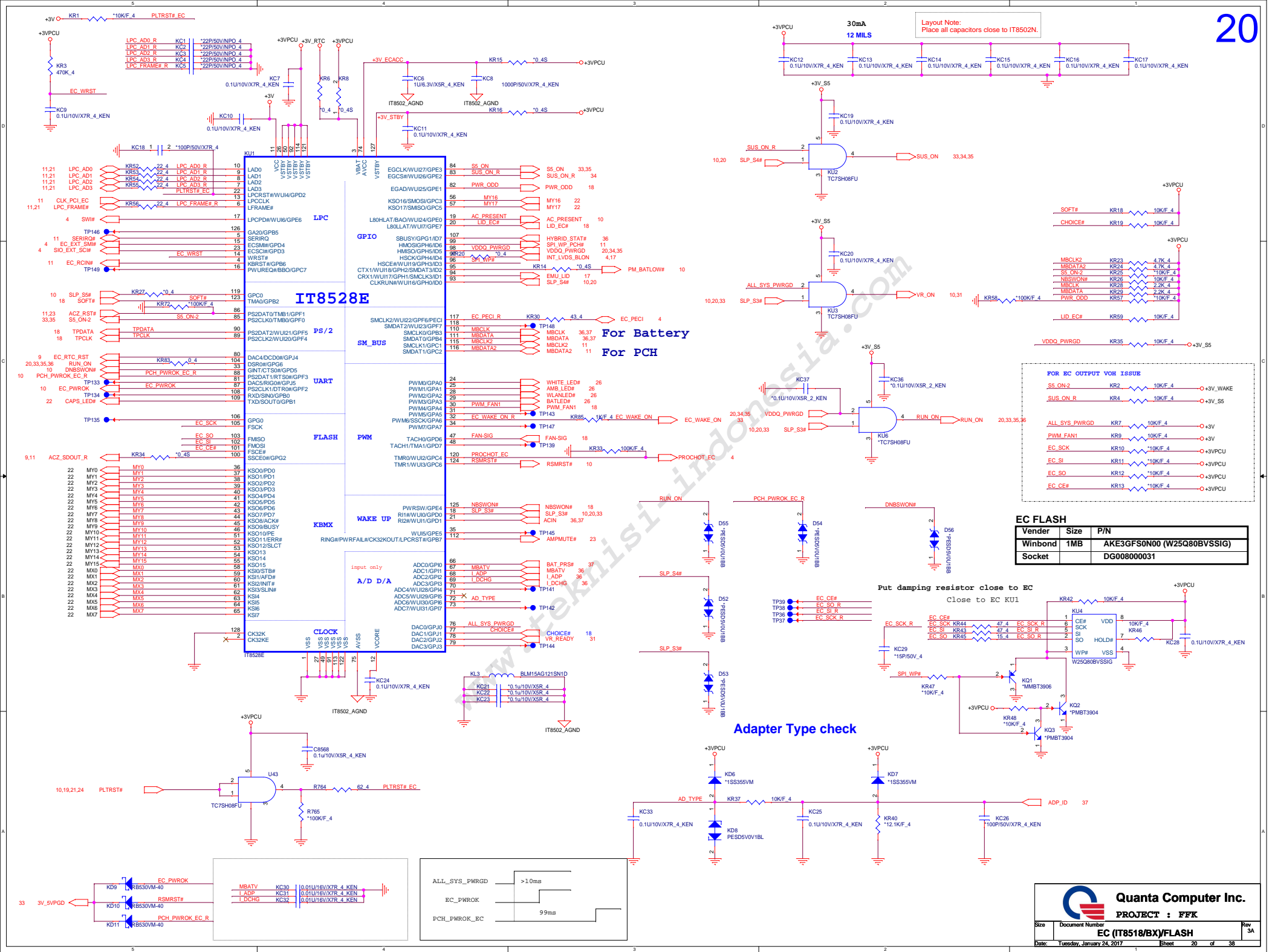
CARD READER

CN27

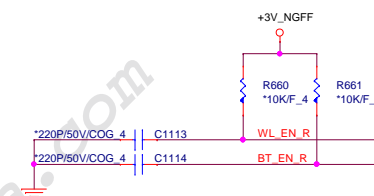
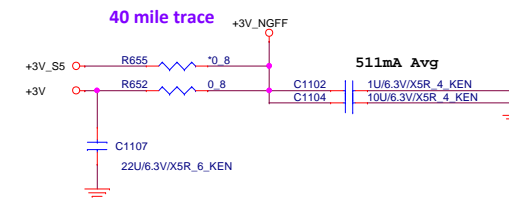
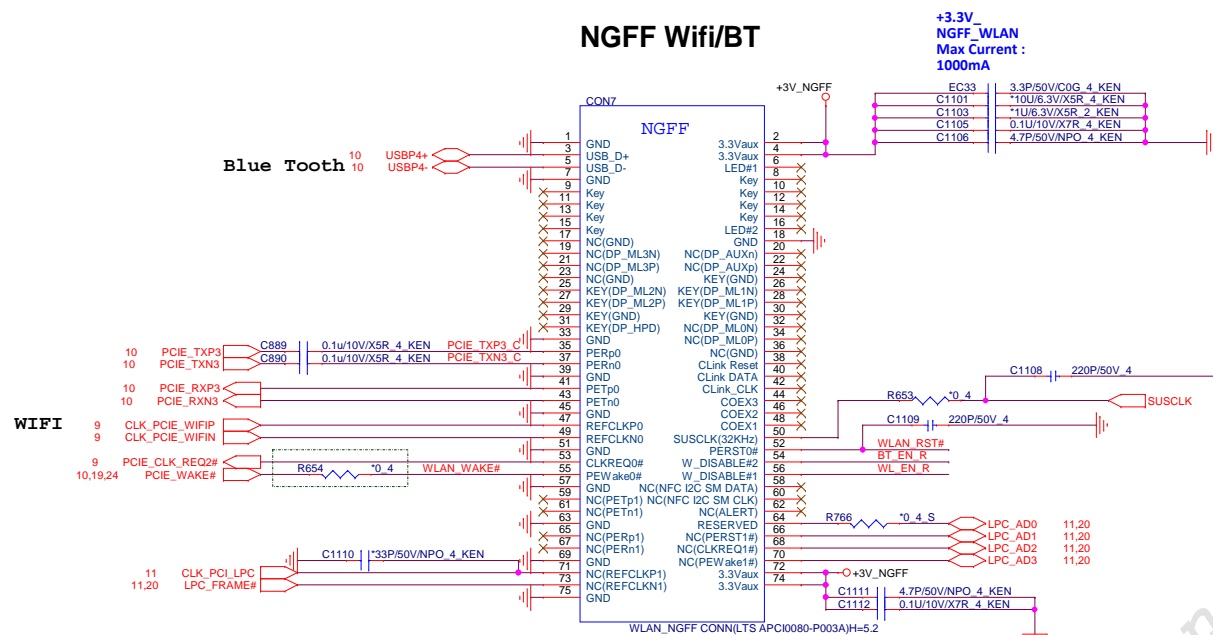
R3X Type

EMI

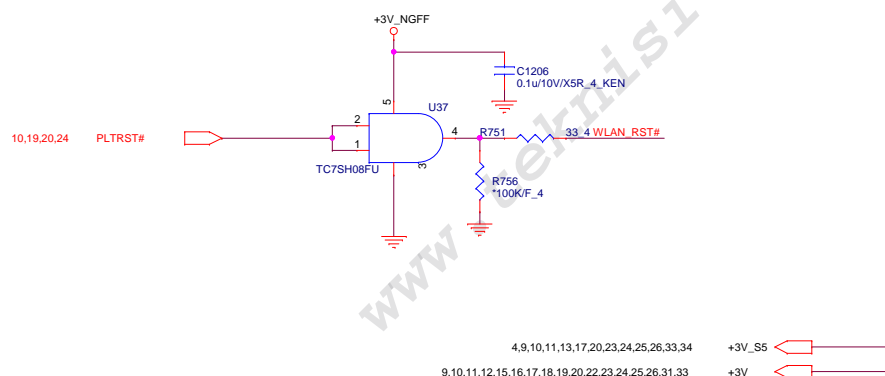




## NGFF Wifi/BT

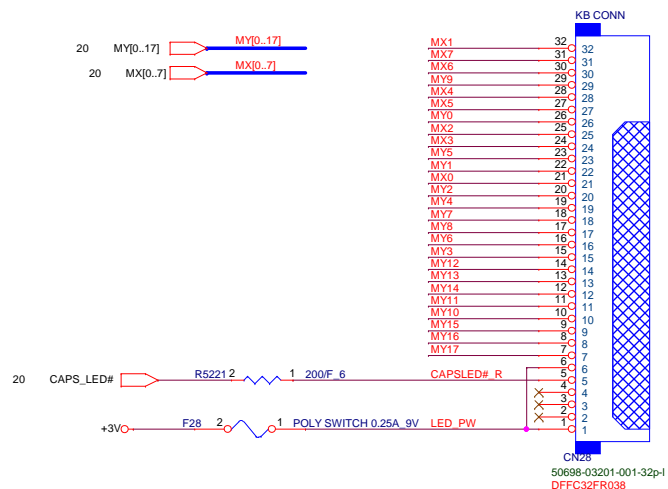


Statement	AC		DC	
	S3	S4	S3	S4
WLAN	X	X	X	X
BT	X	X	X	X

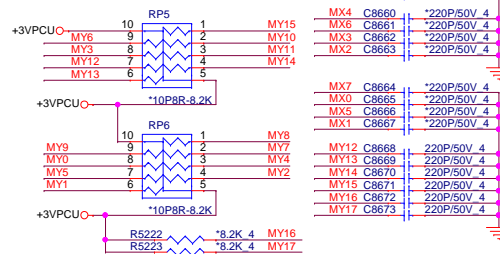


4,9,10,11,13,17,20,23,24,25,26,33,34 +3V\_S5

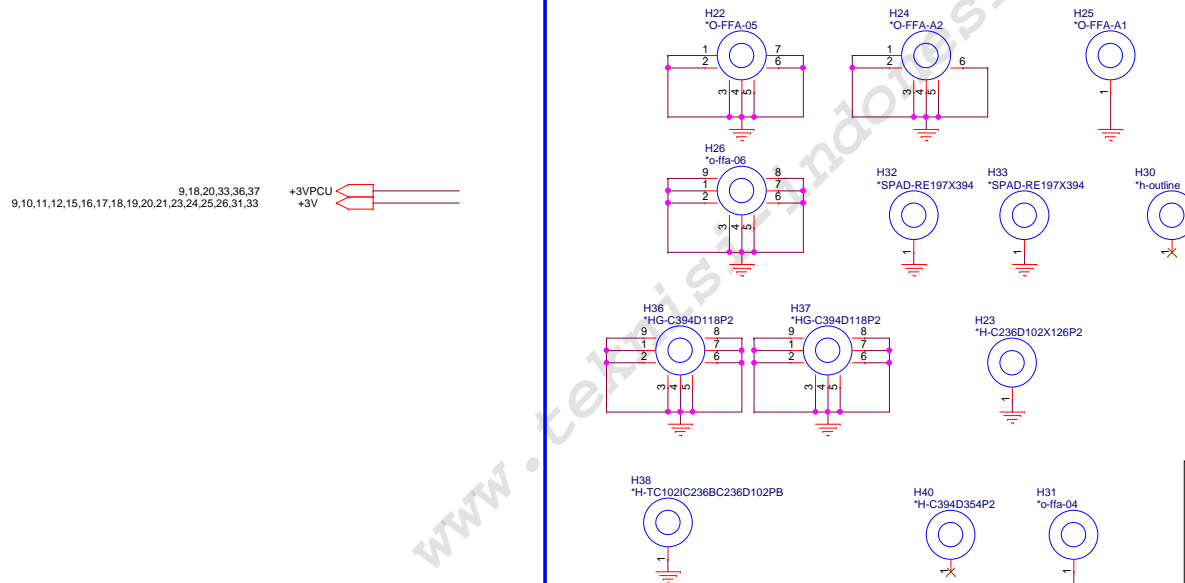
9,10,11,12,15,16,17,18,19,20,22,23,24,25,26,31,33 +3V



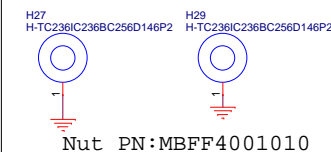
## KEYBOARD PULL-UP



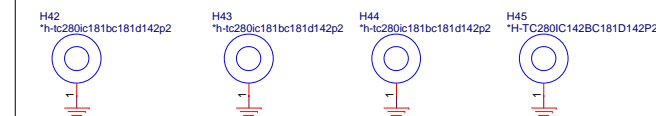
## Hole



## FAN nut



## CPU BLK



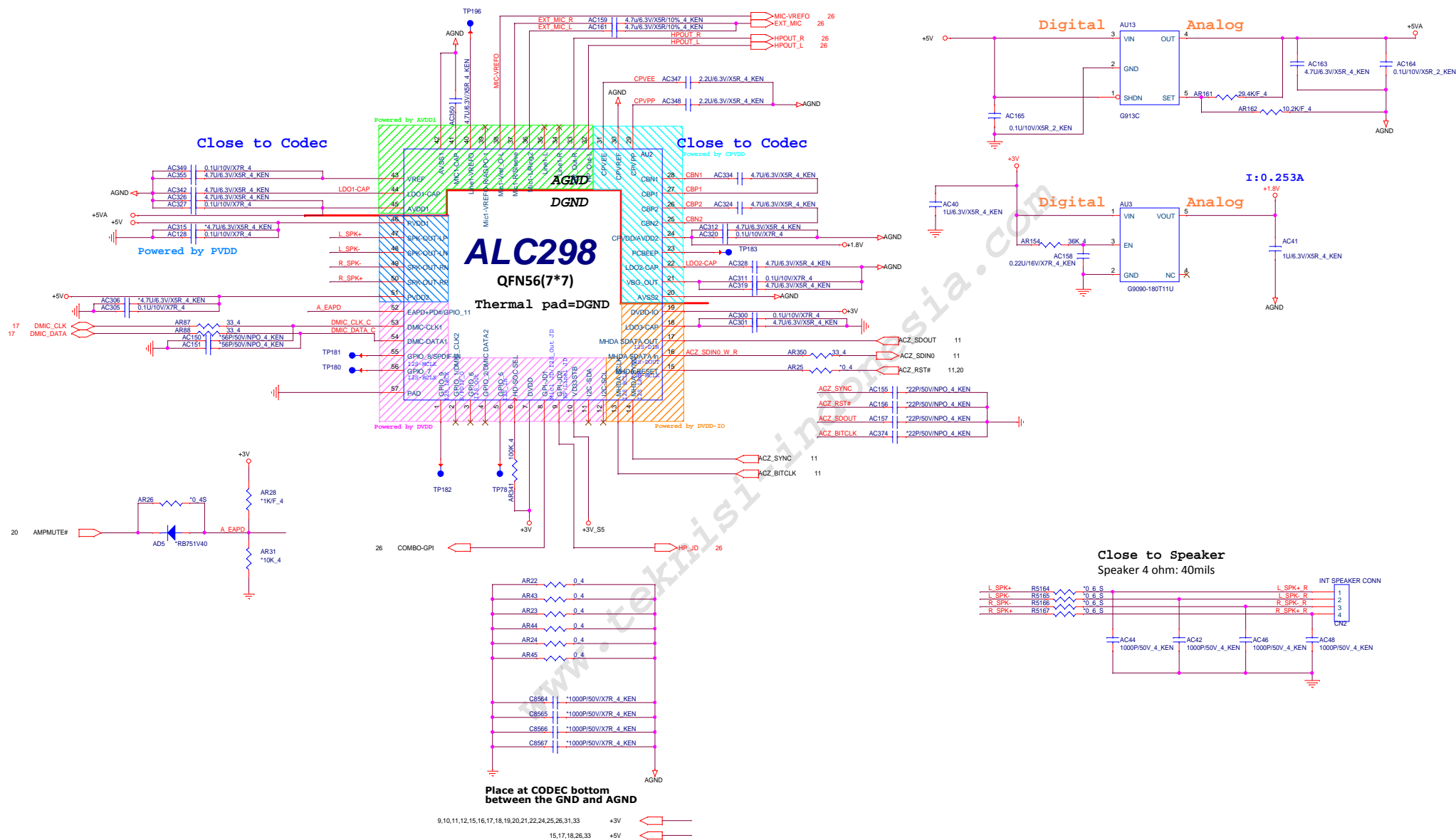
Quanta Computer Inc.

PROJECT : FFK

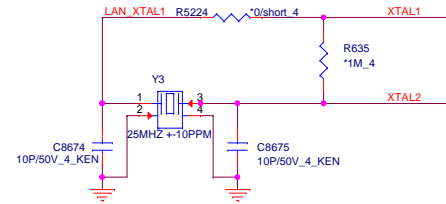
Size	Document Number	Rev
	USB3.0/KB	3A

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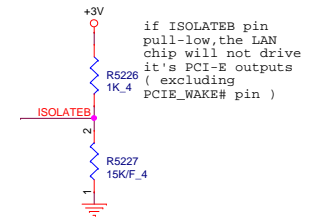
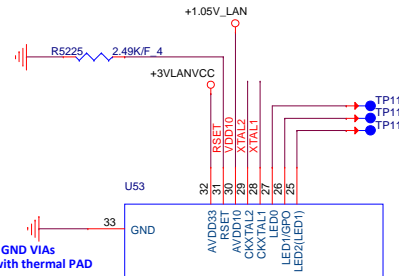
**AUDIO(ALC298-VA0-CG)**



For EMI 0 ~ 22 ohm

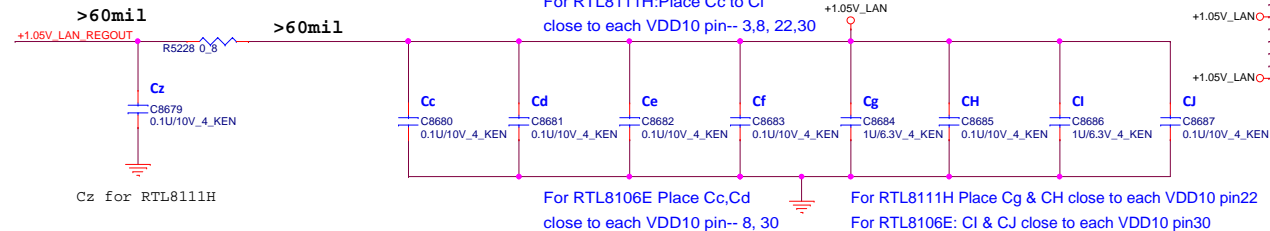


(RTL8106E-CG) 10/100  
AL008106001  
Co-lay  
(RTL8111H-CGT) 10/100/1000  
AL008111011

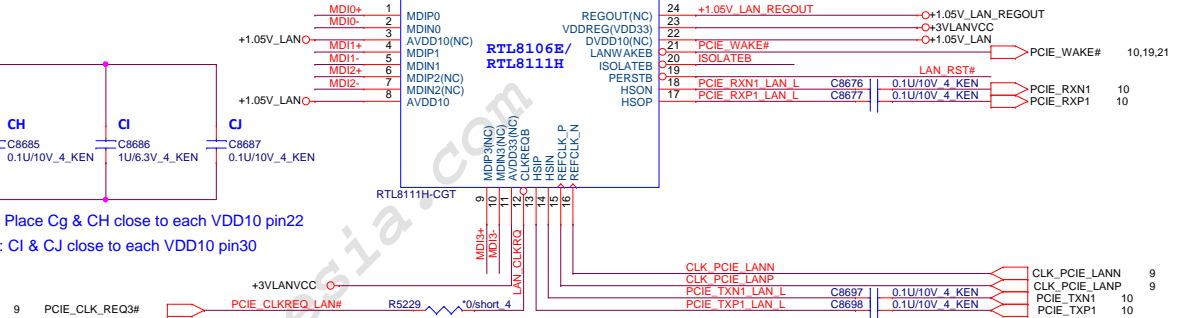


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE\_WAKE# pin)

Trace < 30 mil  
Width > 60 mil  
LDO Mode: Stuff R5228 For RTL8111H  
Power trace Layout 宽度 > 60mil

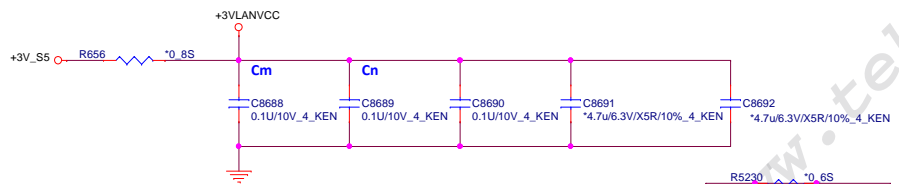


Please add 9 GND VIAS connection with thermal PAD

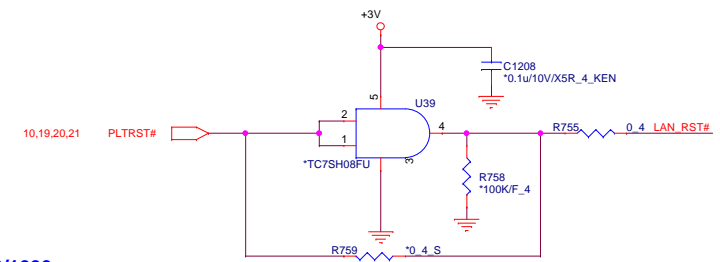


	R5228	Cz C8679
RTL8111H	Add	Add
RTL8106E	NC	NC

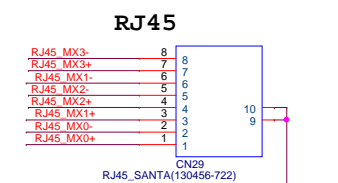
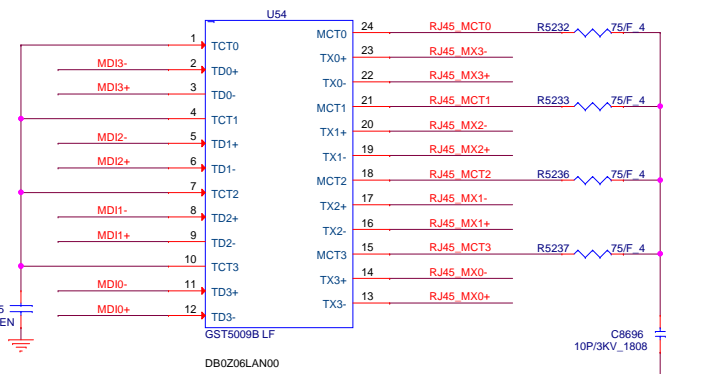
For RTL8111H :  
\*Place Cm and Cn close to each VDD33 pin-- 11, 32  
\*For surge improvement place C8691 and C8692 close to each VDD33 pin-- 11, 32. (optional)  
For RTL8106E : Place Cn and C8690 close to each VDD33 pin-- 23, 32



	U1
10/100 LAN	RTL8106E-CG AL008106001
10/100/1000 LAN	RTL8111H-CG AL008111011



LAN Transformer 10/100/1000



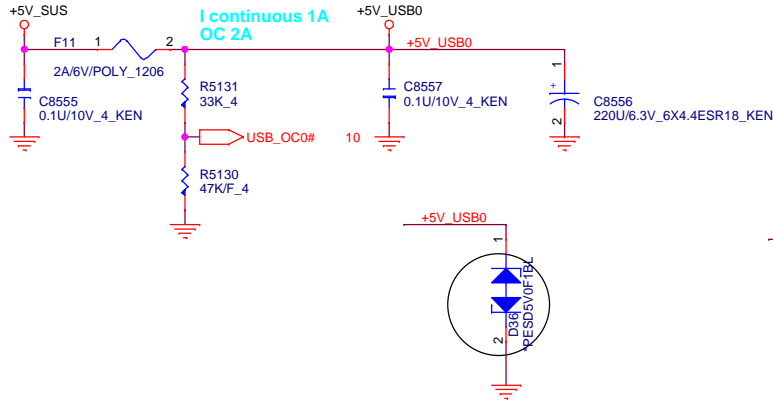
9,10,11,12,15,16,17,18,19,20,21,22,23,25,26,31,33  
4,9,10,11,13,17,20,21,23,25,26,33,34

1000: DB0Z06LAN00  
10/100: DB0EL5LAN00

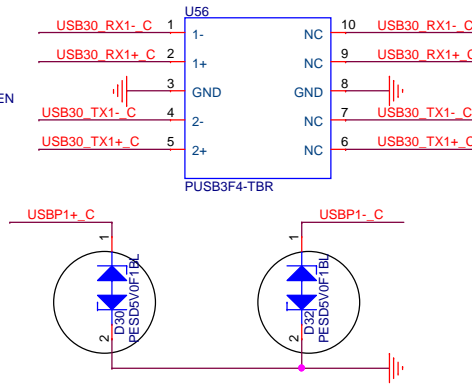


# USB 2.0/3.0 Combo

## USB OCP

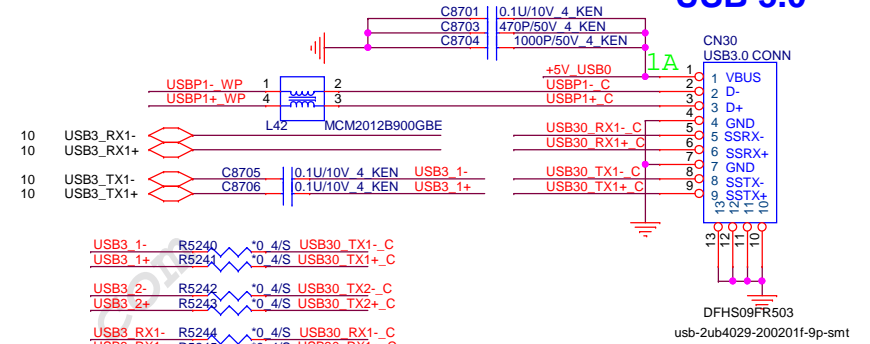


## ESD

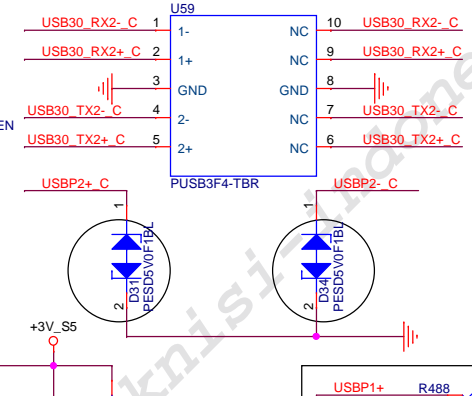
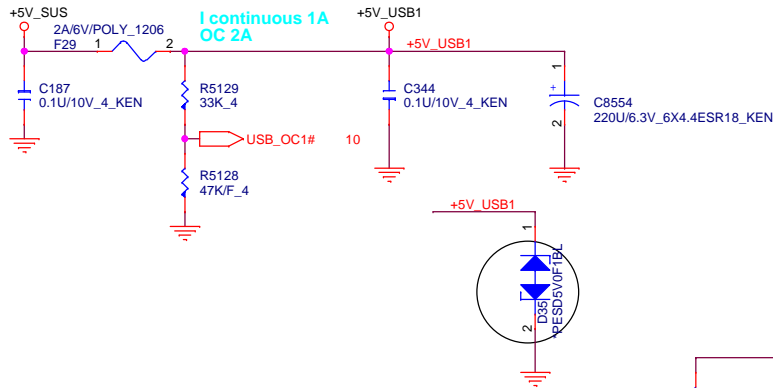


80 mile trace

## USB 3.0

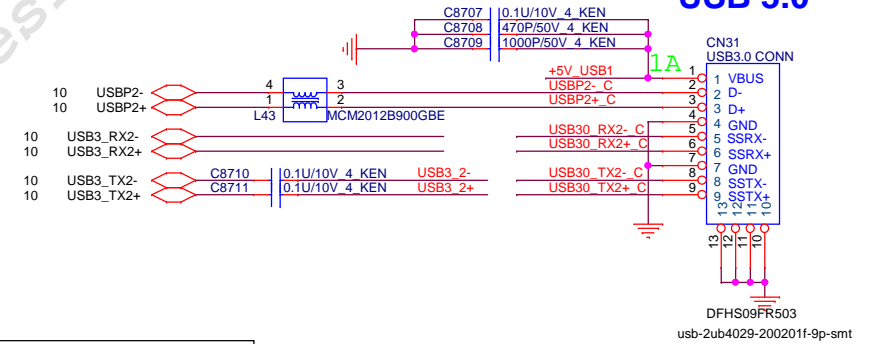


## USB OCP



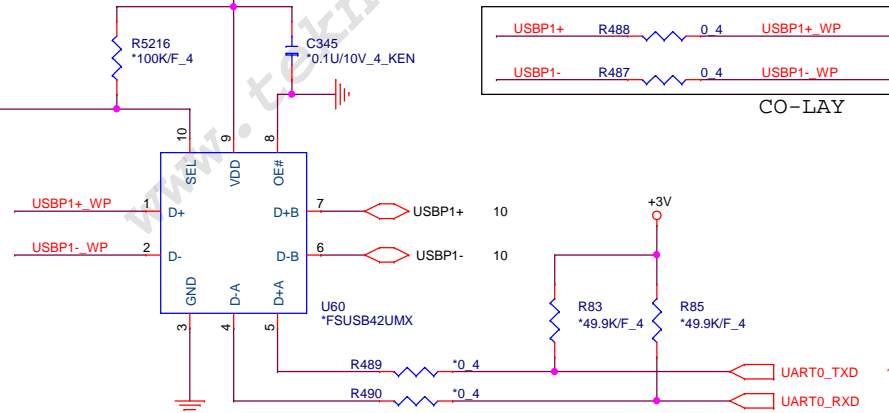
80 mils trace

## USB 3.0



12 USB\_UART\_SEL

/OE	SEL	Function
H	X	I/O=Hi-z
L	L	D(+/-) to D(+/-)A
L	H	D(+/-) to D(+/-)B



CO-LAY

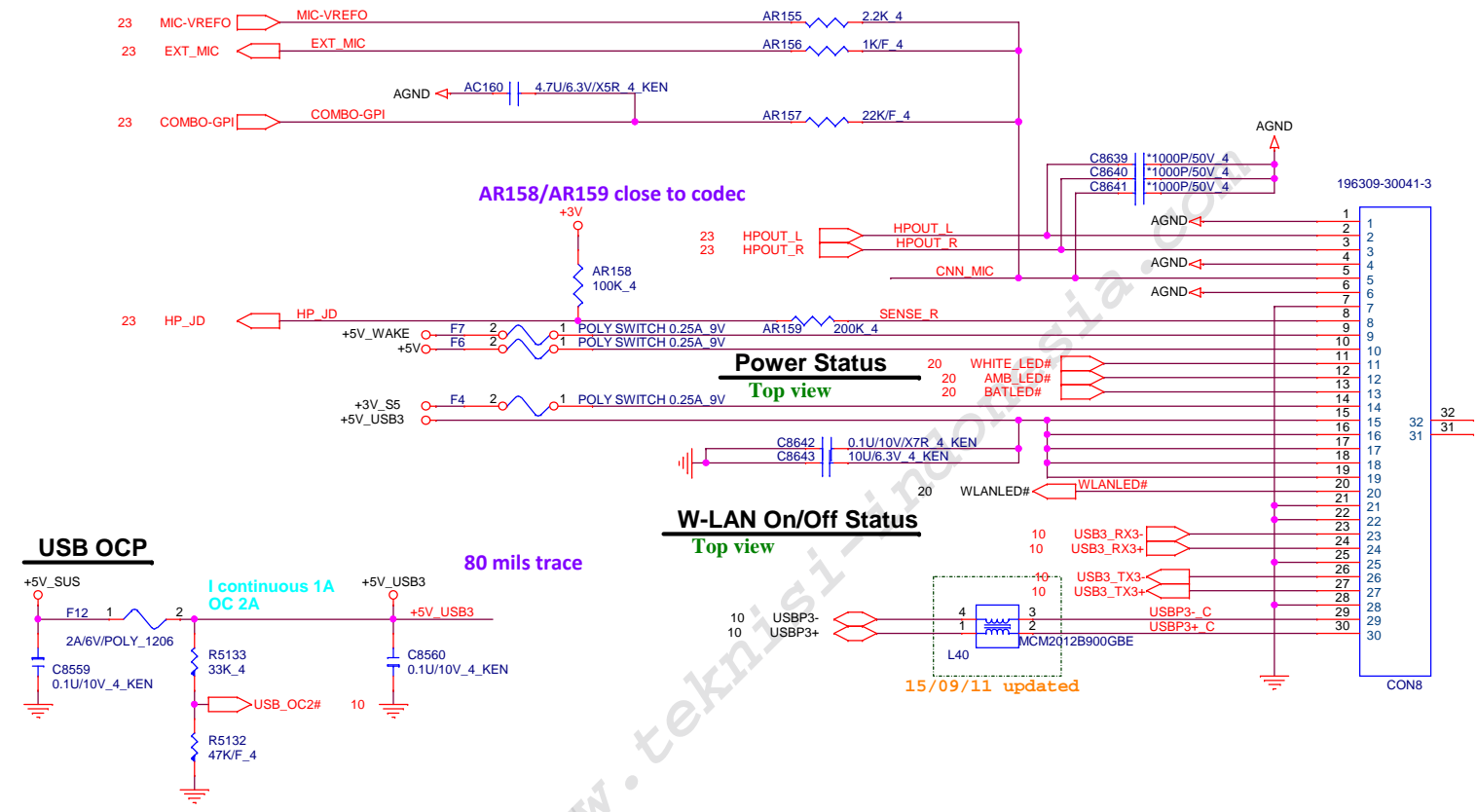
9,18,20,22,33,36,37  
15,26,31,32,33

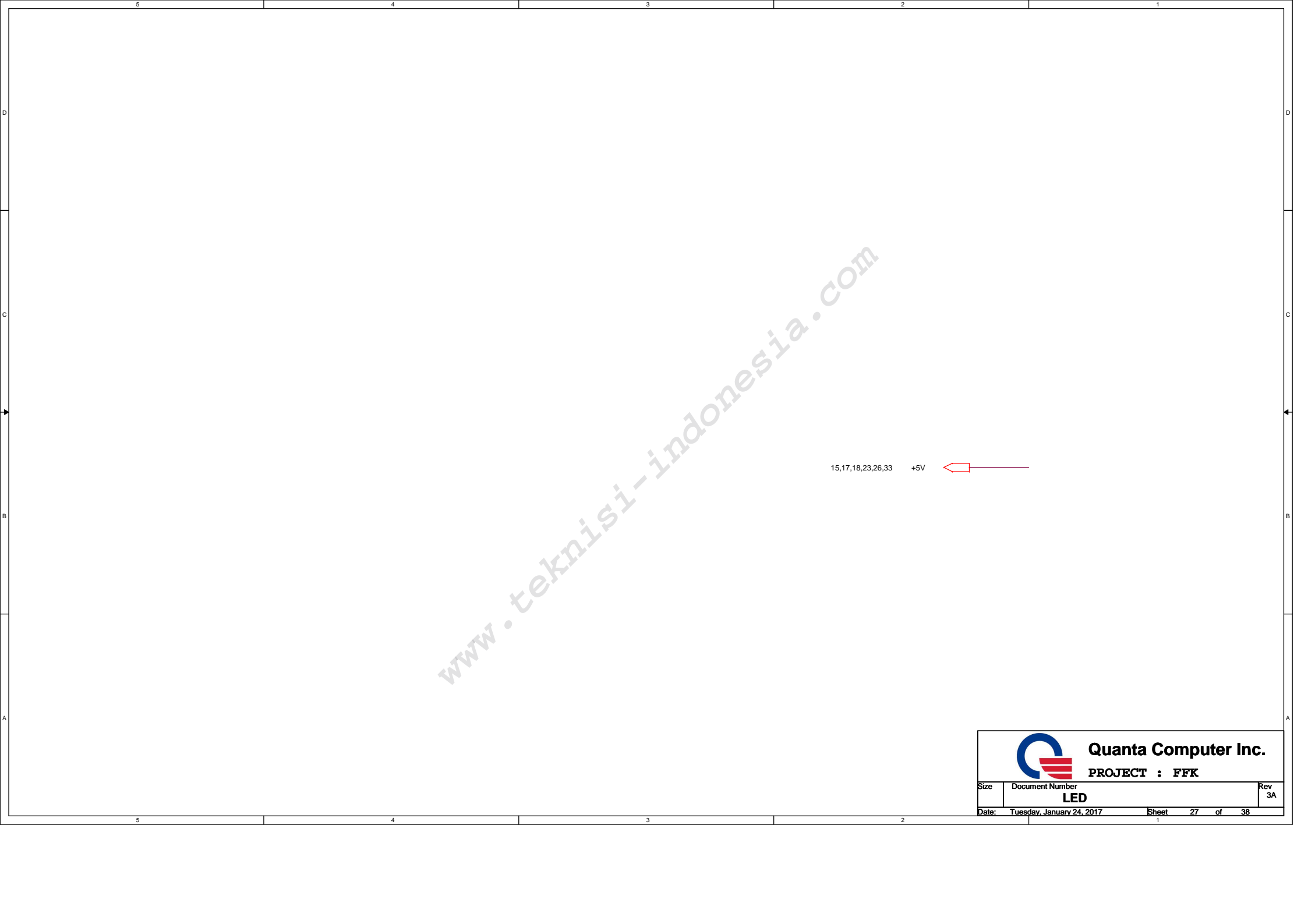


Quanta Computer Inc.

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	USB3.0/KB	3A
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**PROJECT : FFK**

Size	Document Number	Rev
	<b>LED</b>	<b>3A</b>
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OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3		S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L		L	L	L	L	L
+3V	H	L		L	L	L	L	L
+5V	H	L		L	L	L	L	L
+0.6V_DDR_VTT	H	L		L	L	L	L	L
+VCCSA	H	L		L	L	L	L	L
+VCC_GFX	H	L		L	L	L	L	L
+VCC_CORE	H	L		L	L	L	L	L
+1.0V_VCCIO(+1.0V_VCCSTG)	H	L		L	L	L	L	L
SUS_ON	H	H		L	L	L	L	L
+5V_SUS	H	H		L	L	L	L	L
+1.2V_SUS	H	H		L	L	L	L	L
S5_ON	H	H		H	L	L	L	H
+3V_S5	H	H		H	L	L	L	H
+1.0V_S5	H	H		H	L	L	L	H
EC_WAKE_ON	H	H		H	L	H	L	H
+3V_WAKE	H	H		H	L	H	L	H
+5V_WAKE	H	H		H	L	H	L	H


(+1.0V\_S5:For VCCPRIM\_CORE/VCCPRIM\_1P  
/VCCMPHYAON\_1P  
/VCCMPHYGT/VCCAMPHYPLL/  
VCCAPLL/VCCSRAM/VCCCLK1~6)/VCCST/VCCPLL

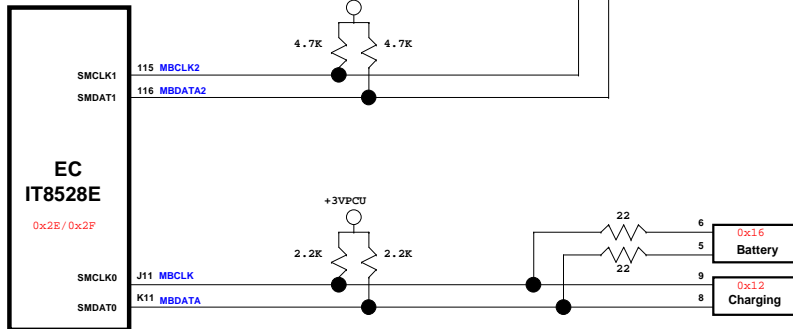
**Resister tolerance:**

F :+/- 1%, (example:69.8K/F\_4)  
others are +/- 5%, (example:69.8K\_4)

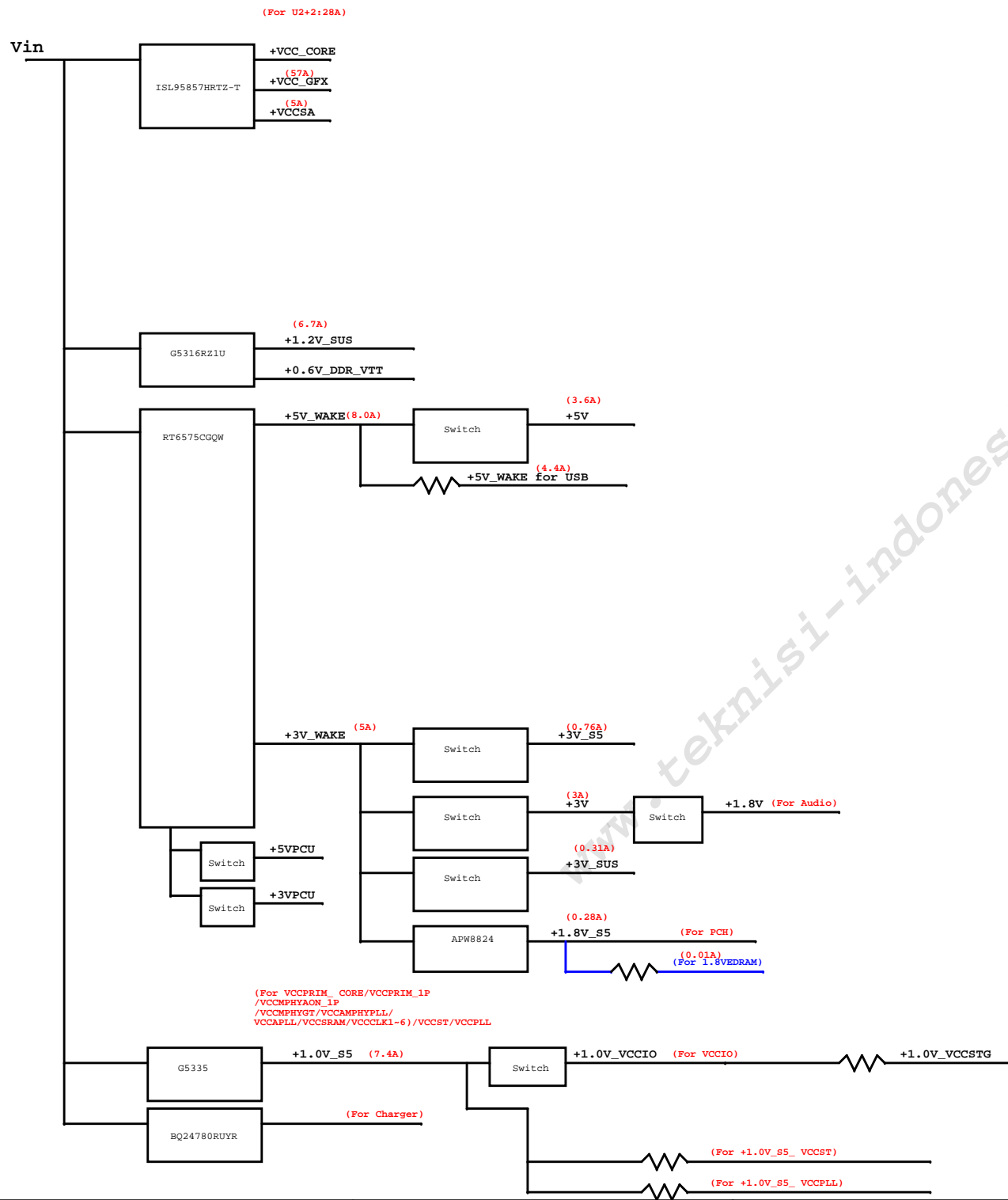
**Capacitor tolerance:**

X7R: +/- 10%  
X5R: +/- 10%  
Y5V: +80%~-20%  
others are +/- 5%

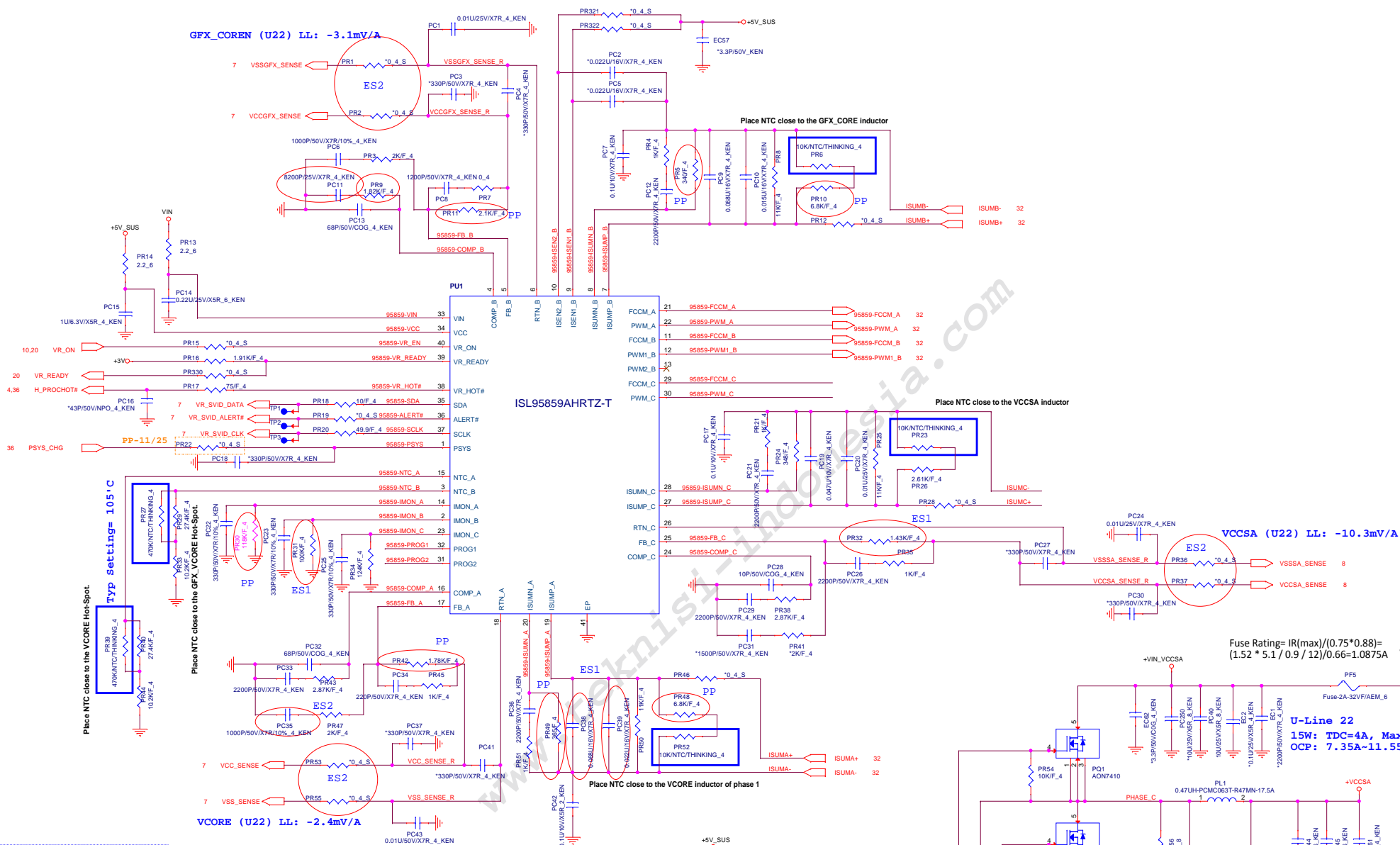
 <b>Quanta Computer Inc.</b> <b>PROJECT : FFK</b>		Rev
		3A
Size	Document Number	
<b>POWER MAP</b>		
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Function	IC	SMBus Address
Thermal IC	NCT7717U	1001000xb (0x90)
Charge IC	ISL88732HRTZ-T	TBD
Battery	Battery	TBD
NFC	TBD	TBD

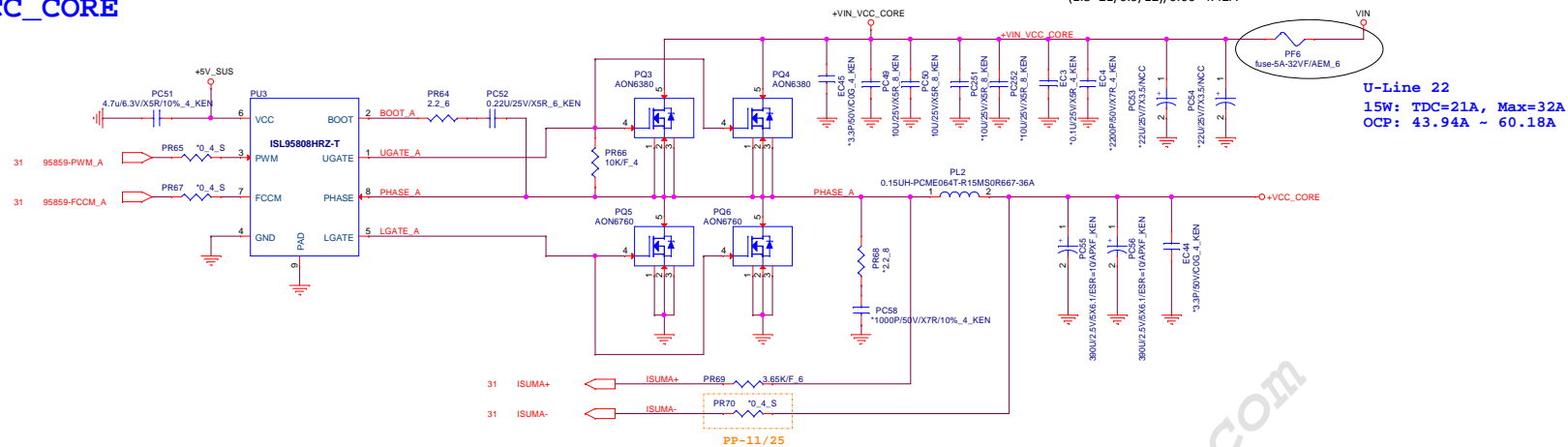


GFX\_CORE (U22) LL: -3.1mV/A



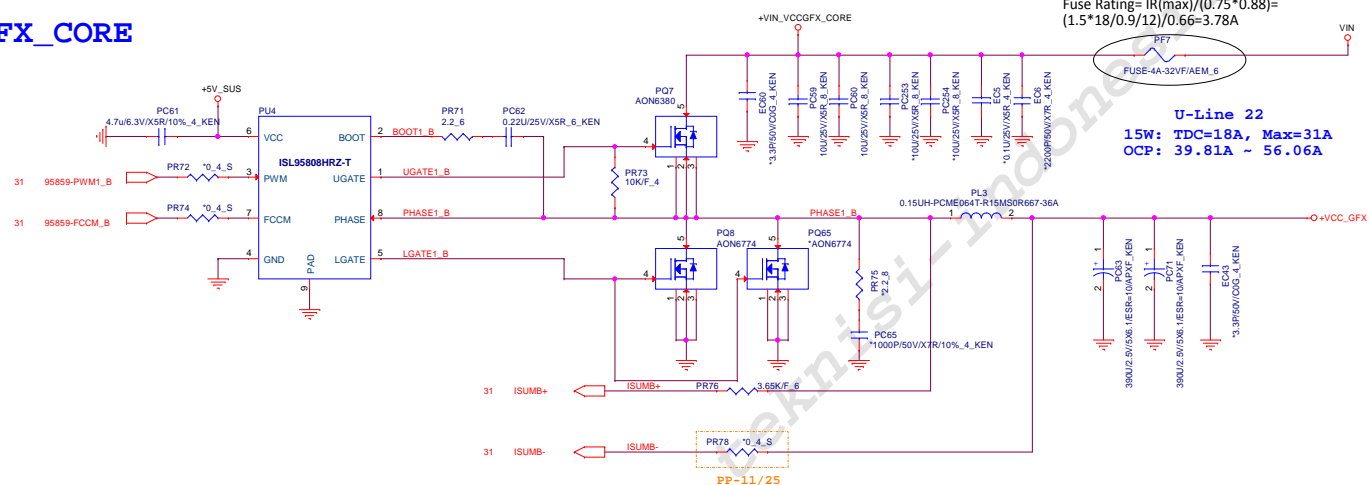
## VCC\_CORE

$$\text{Fuse Rating} = \text{IR}(\text{max}) / (0.75 * 0.88) = (1.5 * 21 / 0.9 / 12) / 0.66 = 4.42\text{A}$$

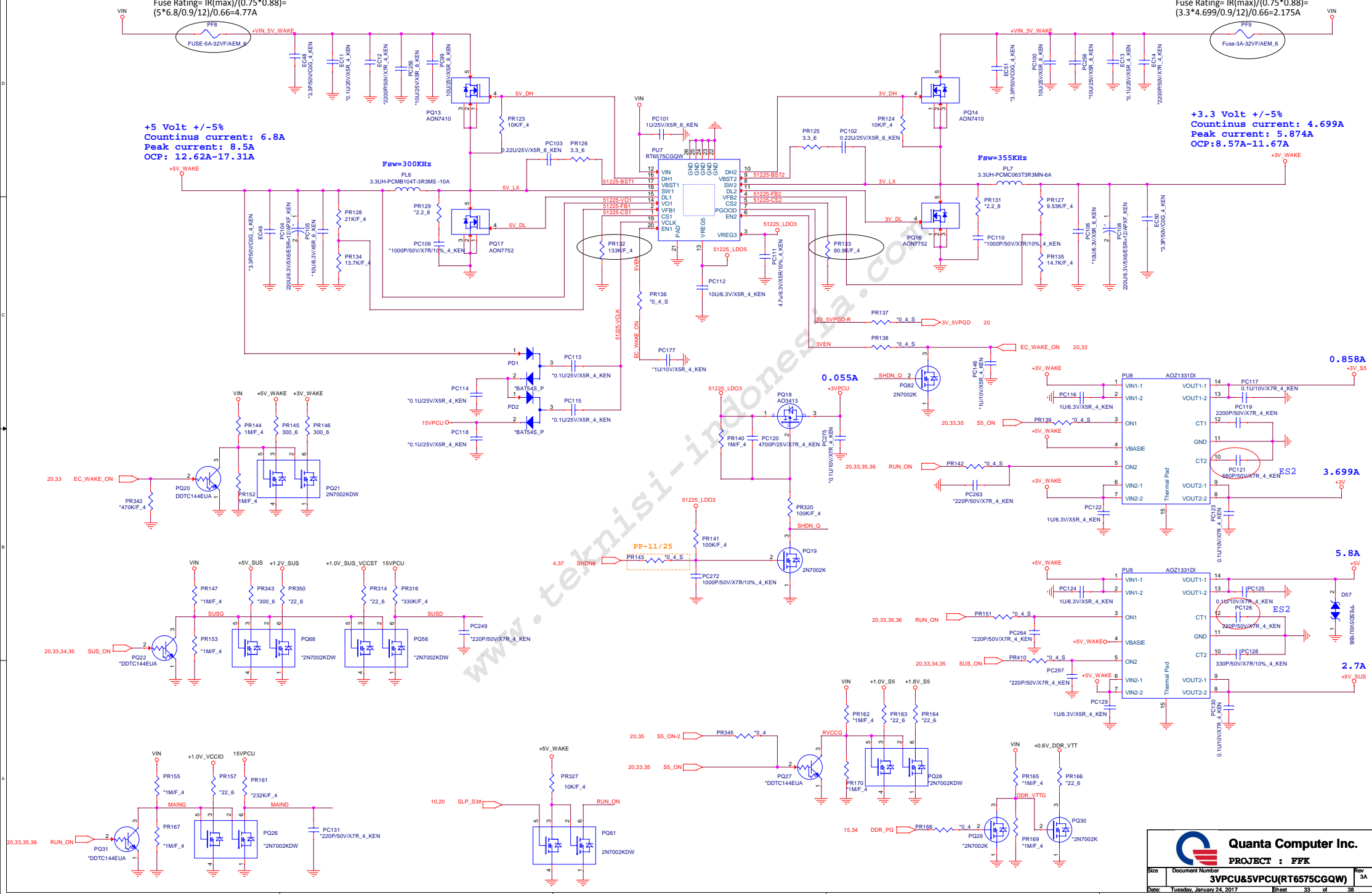


## GFX\_CORE

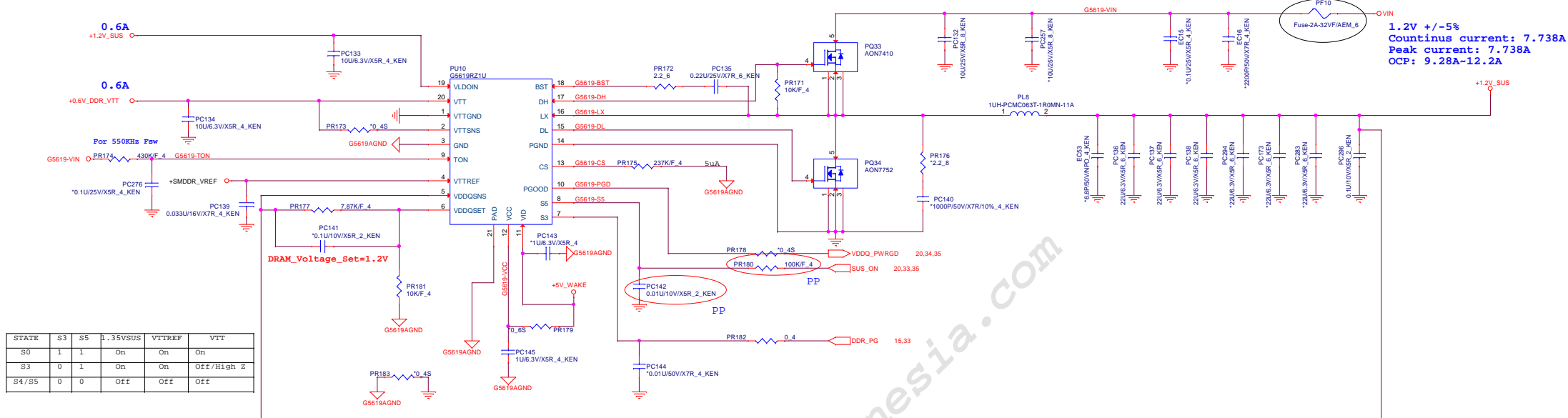
$$\text{Fuse Rating} = \text{IR}(\text{max}) / (0.75 * 0.88) = (1.5 * 18 / 0.9 / 12) / 0.66 = 3.78\text{A}$$



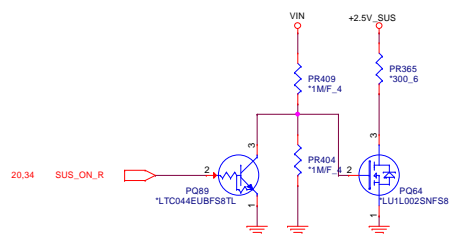
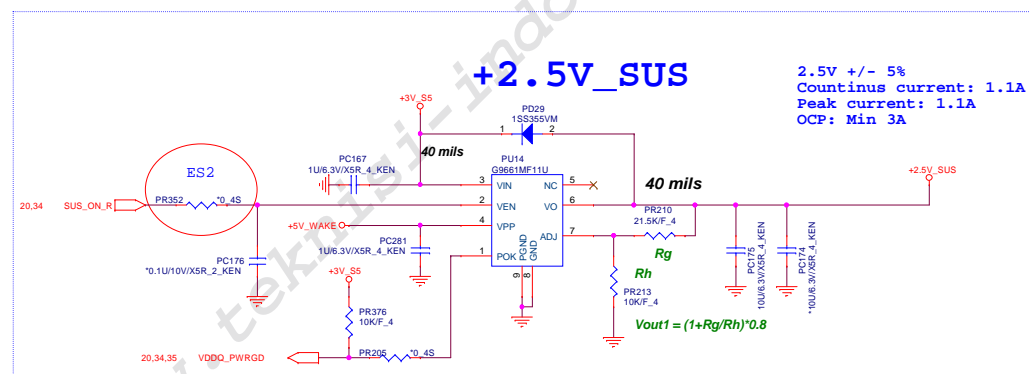


$$\text{Fuse Rating} = I_R(\text{max}) / (0.75 * 0.88) = (3.3 * 4.699 / 0.9 / 12) / 0.66 = 2.175 \text{ A}$$


## 1.2VSUS & VTT\_MEM

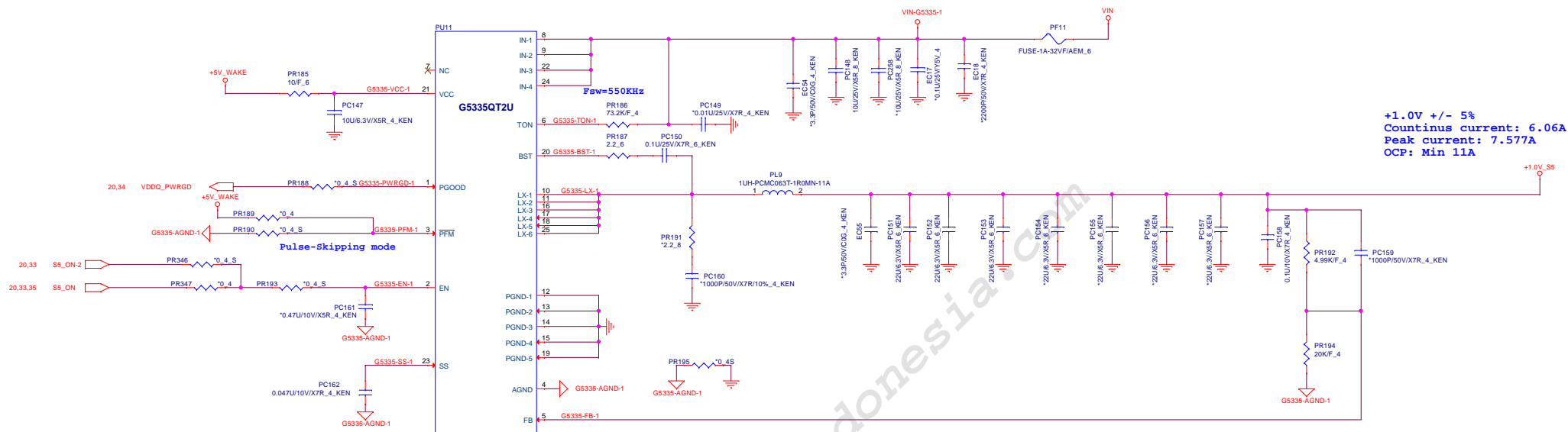
$$\text{Fuse Rating} = I_R(\text{max}) / (0.75 * 0.88) = (1.2 * 7.738 / 0.9 / 12) / 0.66 = 1.3026 \text{ A}$$


STATE	S3	S5	1.35VSUS	VITREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



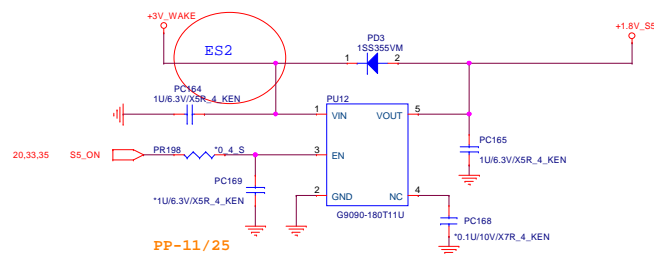
+1.0V\_S5

$$\text{Fuse Rating} = I_R(\max) / (0.75 \times 0.75) = (1.0 \times 6.06 / 0.9 / 12) / 0.66 = 0.85 \text{ A}$$



+1.8V\_S5

1.8V +/- 5%  
Countinus current: 0.217A  
Peak current: 0.217A

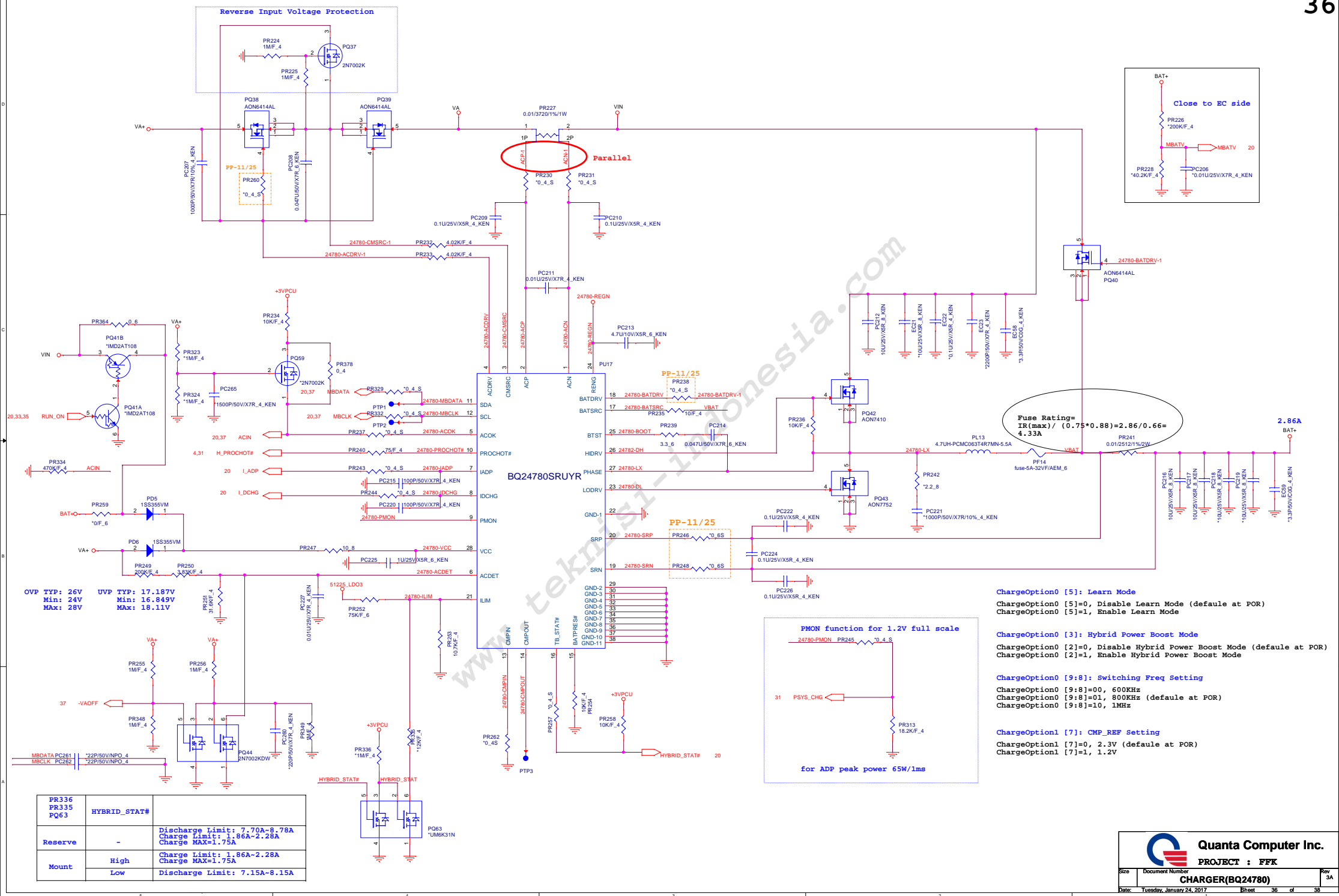


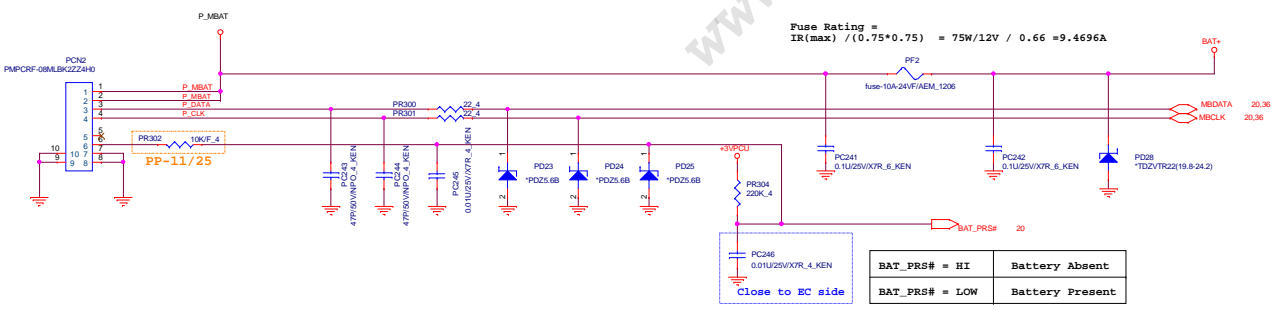
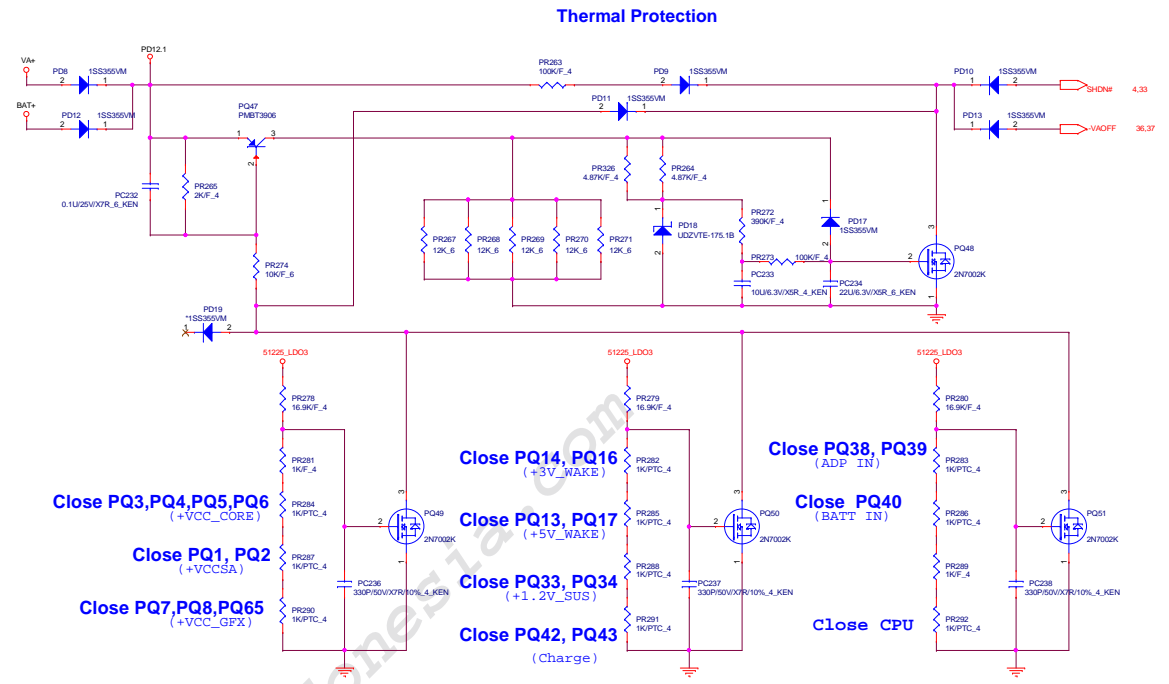
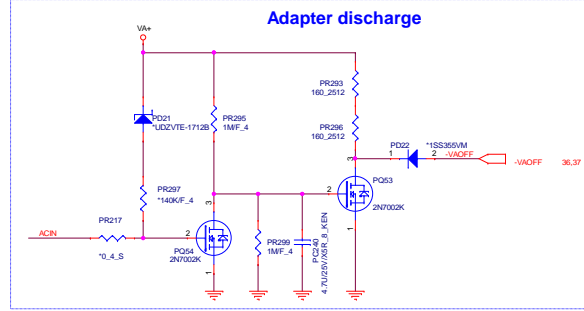
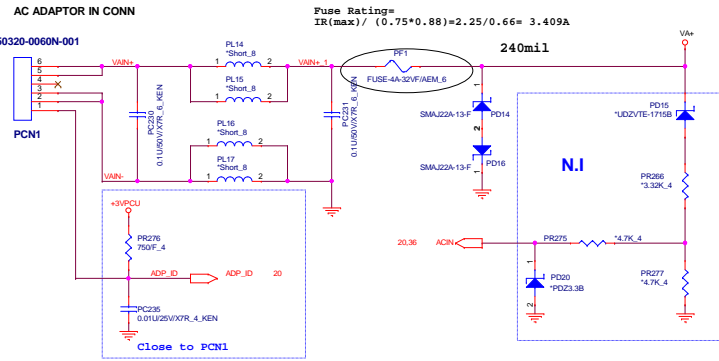
+1.0V\_SUS\_VCCST

+1.0V\_SUS\_VCCST 0.24A

+1.0V\_VCCIO

### 3.1A





### KabyLake ULT Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)

